Internal Report #62
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MJS-CRS
BCE HARDWARE DESCRIPTION

I. General Description

A. Introduction

This plan describes the BCE (bench checkout equipment) for the CRS (cosmic-ray subsystem) to be flown on MJS (Mariner-Jupiter-Saturn). The BCE consists of computer-controlled hardware which will control and support the CRS when it is off the spacecraft. The BCE description may be broken down into three categories:

1) the interface hardware, which will be constructed at Caltech.
2) the computer hardware, or ADPE (automatic data processing equipment).
3) the software or programming.

Since the ADPE and software are described elsewhere, this plan is primarily concerned with a description of the interface hardware.

B. Objectives

The objectives of the BCE may be grouped under four main headings:

1) Acquire and accumulate data from an externally stimulated CRS.

2) Acquire, accumulate, and monitor analog status data.

3) Calibrate PHA's and discriminator thresholds.

4) Perform functional tests of the CRS logic implementation.

Mode 1, acquire and accumulate, is intended to allow the BCE to support calibrations of the CRS with particle beams at accelerator facilities, with radioactive sources, and with ground level muons. In this mode the ADPE sends commands to the CRS, issues word gates, etc. as necessary to read out events, records data on mag tape, and types a summary of the data to the operator.

Mode 2, monitor status, will be active at all times. The ADPE will read analog status data, power supply voltage and current, and temperature probes and will check the value of these parameters. Any significant departures from normal status will cause warnings to be typed and, if warranted, CRS power may be cut off.

Mode 3, calibrate, and mode 4, test, are mutually exclusive since they share the same hardware. In calibrate mode test pulses are connected to the test input of one of the CRS preamps and the appropriate rate scaler or PHA buffer is read out. This process requires that the BCE be able to set the CRS rate multiplexor (mux) to the appropriate rate scaler in a reasonably short time.

In test mode, the ADPE generates events according to a programmed sequence (possibly involving a psuedo-random number generator). The appropriate preamps are triggered and the CRS rate and PHA data are read out and compared with expected response. Deviations are noted for further investigation.

C. General Description of Hardware

The hardware consists of the ADPE and the interface hardware. The interface hardware may be broken down into three modules:

1) The Flight Data System(FDS) simulator and control unit, called the FDC.

2) The calibration mode stimulus module, called the Cal Stim.

3) The functional test mode stimulus module, called the FT Stim.

The breakdown of the BCE hardware into these categories is illustrated in Figure 1.

A brief overall description of the BCE hardware is presented here; a more detailed description of each of the hardware categories is given in following sections.

The FDC will, under ADPE control, generate and receive most of the CRS/FDS signals. These signals are tabulated in Table 1. A more complete description is in the FDS memo. Signals received from the CRS will be formatted and sent to the ADPE. The FDC will also control the state of the CRS rate multiplexor and the CRS power.

The Cal Stim will generate a precision analog test pulse which will be manually connected to the appropriate CRS preamp test input. The rate and amplitude of this pulse is under ADPE control. In addition two coincident pulses with fixed amplitude are generated and used if necessary to satisfy CRS logic requirements for particular rate scalers or PHA buffers.

The FT Stim module will generate up to 50 independent pulses at the 50 CRS preamp test inputs. These pulses have up to 3 possible amplitude states (or four states if zero amplitude is counted). The FT Stim shares

the pulse rate control unit of the Cal Stim. In addition, the same 50 ohm coax lines are used to connect either the Cal Stim or the FT Stim to the CRS test inputs.

D. General Description of Software

The software will be programmed in the FORTH language. Appropriate vocabulary for the four modes of operation specified in section I.B. will be provided. The high-level language features of FORTH should allow easy modification of extension of software when unforeseen situations arise.

II. Interface Hardware

A. FDS Simulator and Control Unit

The FDC is illustrated in Figure 2. It supports all functions of the FDS. It also controls CRS power, controls the state of the rate multiplexor, and includes registers which duplicate the state of the CRS multiplexors. Signal conditioning of analog signals is done in the FDC.

As seen in Figure 2, the FDC can be broken down into several sub-modules which are logically more-or-less separate. These will be described at this point.

The command sub-module receives a 12-bit parallel command word from the ADPE. It generates a command word gate (CWG) and feeds the command to the CRS in serial fashion. A signal (CWF) is also sent to the ADPE to acknowledge receipt and transmission of the command.

The digital information sub-module receives serial digital data from the CRS and converts the date to parallel for the ADPE.

Word gates, redundancy selection, various discrete commands, and power on/off control are handled by the digital control-status hardware. This hardware includes a register which may be read by the ADPE at any time to determine what type of data was most recently received by the digital information sub-module, i.e., whether it was status, rate, or pulse-height data, which of the 4 pulse-height words it was, whether it was read through the A or B redundant lines, and what the state of the rate multiplexor is.

Word gates - PWG, RWG, SWG - are generated in one of the eight formats listed in Table 2. The format is selected by the ADPE. Due care must, of course, be taken to satisfy the timing requirements specified in the FDS memo. Note that once the word gate sub-module is placed in one of the eight possible modes, no further interaction with the ADPE is required until the mode is to be changed.

The signals CLS, HVN, SLR, AMS, and AMR are generated with the proper timing by the FDC whenever required by the corresponding signal from the ADPE. The non-FDS signals SRE, SRM, HCR, PWR, and SLE are generated in the same manner.

An analog information sub-module handles the conditioning necessary between the analog to digital converter in the ADPE and the various analog signals of interest which are listed in Table 1.

Note that the signals for which transmission of a zero can cause a change of state must have associated enable bits, e.g., if the three bits that specify the word gate mode are all zero, does that mean change to mode zero, or does it mean no change from current status? This question is settled by the enable bit, which must be on before any change will take place.

All I/O to the CRS except power is through an I/O unit copied from the JPL FDS I/O unit specifications. Figures 3 and 4 give details of the power system and the I/O unit.

The rate mux in the CRS includes two separate counters-- a 16 - state mux which specified which rates are fed to the accumulators and a 30 - state mux which specifies which rate buffer is being read out. The 30 - state counter serves some additional functions; when the counter overflows from the 30th state to the first, a pulse is generated which transfers the contents of the rate accumulators to the rate buffers and initiates the 24 - to 12 - bit compression, increments the 16 - state rate mux, and increments the digital status mux.

The SRM signal is used to freeze the 16 - state rate mux, but the 30 - state mux must be allowed to increment normally with each RWG so that the transfer and compression will take place. The possibility of adding a BCE - controlled signal which would cause the transfer was considered and rejected on the basis of possible impact on CRS reliability.

B. Calibration Mode Stimulus Module

The Cal Stim is schematically illustrated in Figure 5. The pulse generated for calibration is controlled in amplitude by a 14-bit DAC used as a reference voltage by the pulse generator and a 4-bit, ADPE-controlled attenuator. The dynamic range necessary for discriminator thresholds and PHA ranges is listed in Table 6, which gives threshold and full scale energies, and selected calibration pulses, together with the corresponding voltages needed at the test inputs. Values of the feedback test capacitors are also listed. Absolute accuracy of the calibration should be better than 1% with a goal of 0.3%; repeatability should be better than 0.2% with a goal of 0.05%. In addition to the calibration pulses, two (possibly more) pulses are generated to be used in satisfying CRS coincidence requirements when necessary. ADPE control of the amplitude of these signals is not provided. These signals will normally have constant, fixed amplitude since they are added to the calibration pulse by the CRS slant-discriminator circuitry. The operator can assume manual control over the amplitude of these signals.

For an example of the normal use of the two fixed amplitude pulses, consider the calibration of the LET I slant discriminator. The calibration pulse would be put into the L1 preamp. The two coincidence pulses would be put into L2 and L3. Thus an L1 L2 L3 coincidence is generated and if the calibration signal is high enough the slant will be triggered and the event will be counted by the R18 rate scaler. The actual threshold of the slant is calculated from the amplitudes of the three signals, not from any one.

The Cal Stim module sends a specified number of pulses at a specified rate under ADPE control. After this number of pulses is sent the ADPE is signalled (by PLD) to read out the necessary data from the CRS.

The DAC has a sign bit (30R14) in addition to the 14 amplitude bits; it must always be set (1). The 4 attenuator bits control 3 factor-of-eight dividers and 1 factor-of-four dividers as noted below

Bit No.	Att. factor
40RØ	8
40R1	8
40R2	8
40R3	4

The pulse rate control uses 2 bits (CRC) to select one of four possible rates:

CRC	Rate
00	14400/8 = 1800 cps
01	14400/15 = 960 cps
10	14400/33 = 436 cps
11	14400/191 = 75 cps

C. Functional Test Mode Stimulus Module

The FT Stim is illustrated in Figure 5. Fifty gates are connected between a pulse bus and the fifty preamp test inputs. Each of the fifty gates may be independently controlled. The gates provide the ADPE with some control over pulse amplitude. Table 3 lists the possible states of each gate. Figure 6 shows details of a gate. Figures 7a and 7b show locations on the 2-D plots which can be pulsed by the FT Stim. Drifts in these locations of up to 5-10% can be tolerated.

Note that the gates actually have other, non-independent states.

Control of the gates is effected through a 150-bit register that may be filled serially with 10 16-bit words from the APDE. The 10 least significant bits of the first of these 10 words are shifted of the end of the register. Table 3 gives the correspondence between bits and states of the gates. After completion of pulses as specified in number and rate by the control, the FT Stim returns a signal to the APDE to read out the necessary data from the CRS.

III. ADPE and ADPE Interfaces

The ADPE (See Figure 1) consists of a PDP-11/10 computer with the following peripherals:

DEC core memory - 8K words.

TI KSR-733 terminal.

LSi ADM-1 CRT terminal

AED 2500 floppy disk system.

Kennedy 9700 mag tape system.

DEC AR-11 analog subsystem

DEC KW-11 L 60-Hz clock.

2 DECkit 11H parallel digital interfaces.

The TI terminal consists of a keyboard and a 30 character-per-second thermal printer. It uses special, 8 1/2" wide paper. The unit is quiet, light-weight, and portable.

The terminal will be used to display large amounts of rapidly changing data, such as the rate block. It may also be used to display status and for warnings. The display will show 24 80-character lines. A printer interface will be added to allow use of the GSFC Versatec printer for hard copy.

The AED floppy disk has a capacity of 128K words, a maximum transfer rate of 15,625 words/sec, and a maximum access time less than 650 m sec.

The Kennedy tape system uses 600 foot reels of mag tape. It is a single drive system with a drive that requires only 8 3/4" of rack space and that weighs less than 40 pounds.

The 60-Hertz clock generates interrupts 60 times per second if enabled.

The DECkit interfaces are parallel 16-bit interfaces. Each of the two kits has four 16-bit output registers and four 16-bit input receivers.

An interrupt may be generated by the external device on the input lines. The output, but not the input, words are buffered with flip-flop registers. Table 4 shows the tenative allocations of the interface lines.

The AR-11 analog subsystem includes a 16-channel, 10-bit ADC, a programmable real-time clock and 2 DAC's. It will be used to measure the analog voltages (power supply, thermistors, analog data) provided by the FDC and CRS. The real-time clock is used to generate interrupts after computer-controlled periods ranging from ~ 10 μ sec to 2.56 sec.

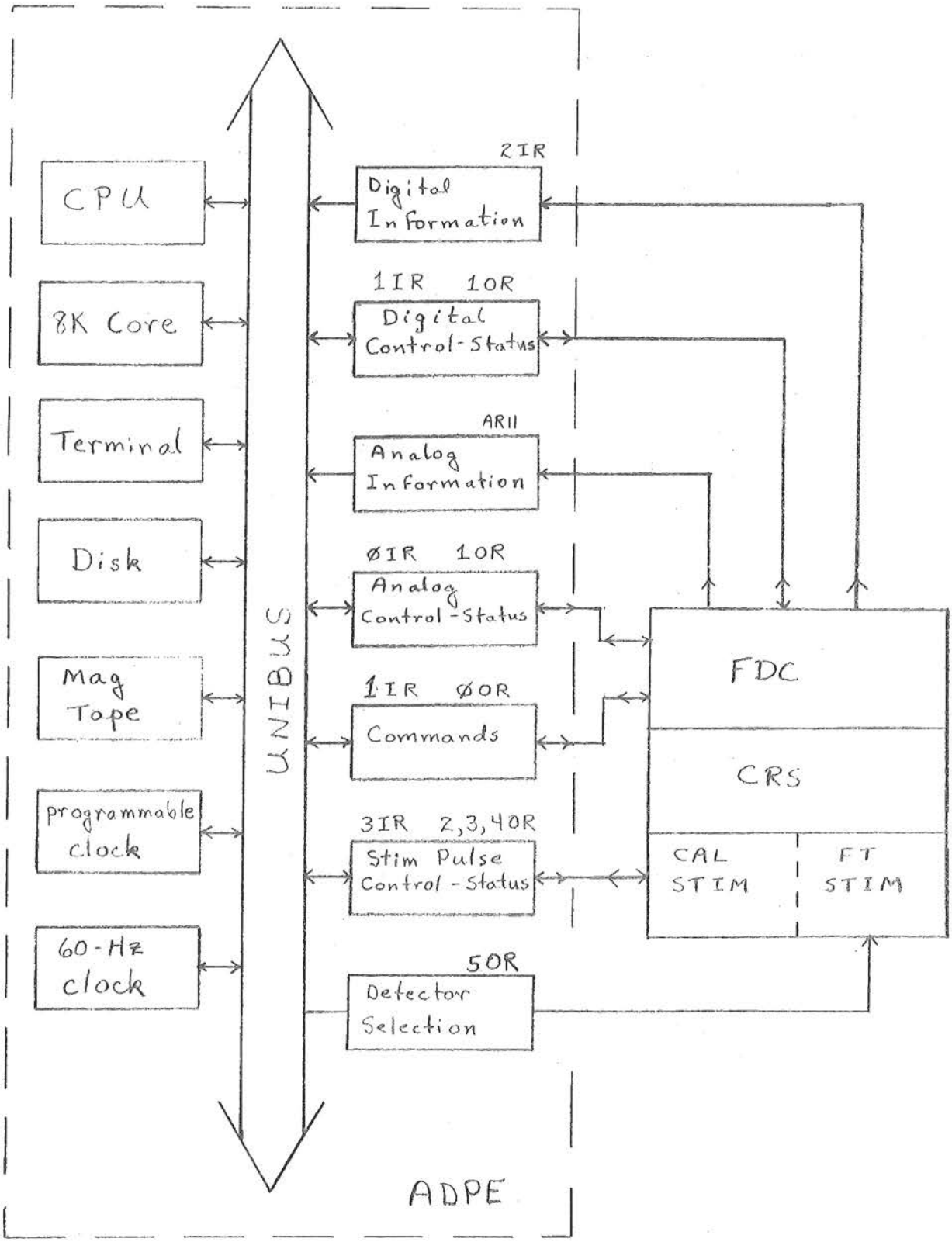


Figure 1. RCE System Block Diagram

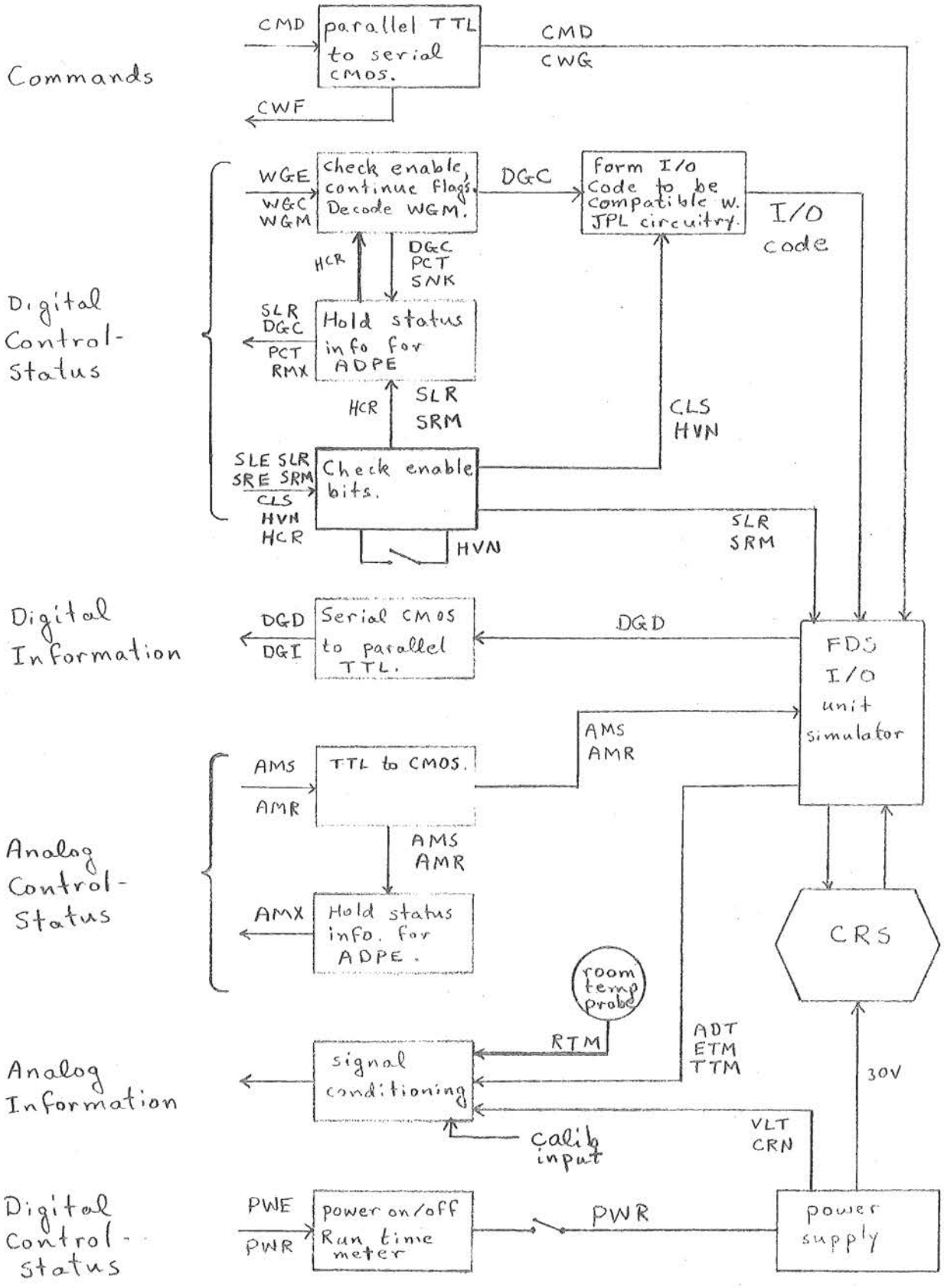

Commands
CMD
parallel TTL to serial CMOS.
CMD
CWG
CWF
Digital Control-Status
WGE
W&C WGM
check enable, continue flags. Decode WGM.
DGC
form I/O Code to be compatible w. JPL circuitry.
I/O code
HCR
DGC PCT SNK
SLR DGC
PCT RMX
Hold status info for ADPE
HCR
SLR SRM
CLS HVN
SLE SLR SRE SRM
CLS HVN HCR
Check enable bits.
HVN
SLR SRM
Digital Information
DGD
DGI
Serial CMOS to parallel TTL.
DGD
FDS I/O unit simulator
AMS AMR
Analog Control-Status
AMS
AMR
TTL to CMOS.
AMS AMR
AMX
Hold status info. for ADPE.
CRS
room temp probe
RTM
ADT ETM TTM
Analog Information
signal conditioning
30V
calib input
VLT CRN
Digital Control-Status
PWE
PWR
power on/off Run time meter
PWR
power supply

Figure 2. FDC

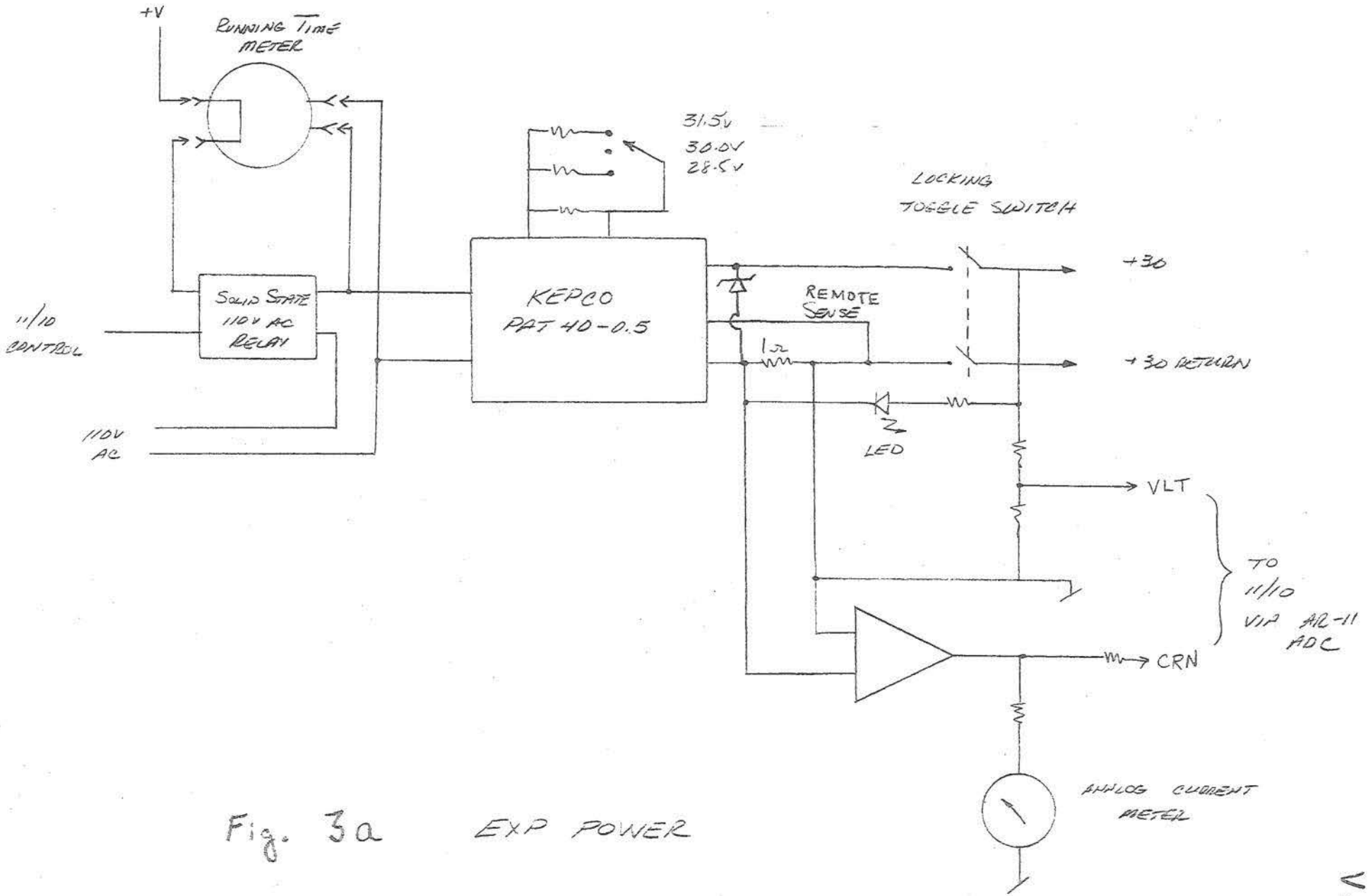


Fig. 3a EXP POWER

V.3

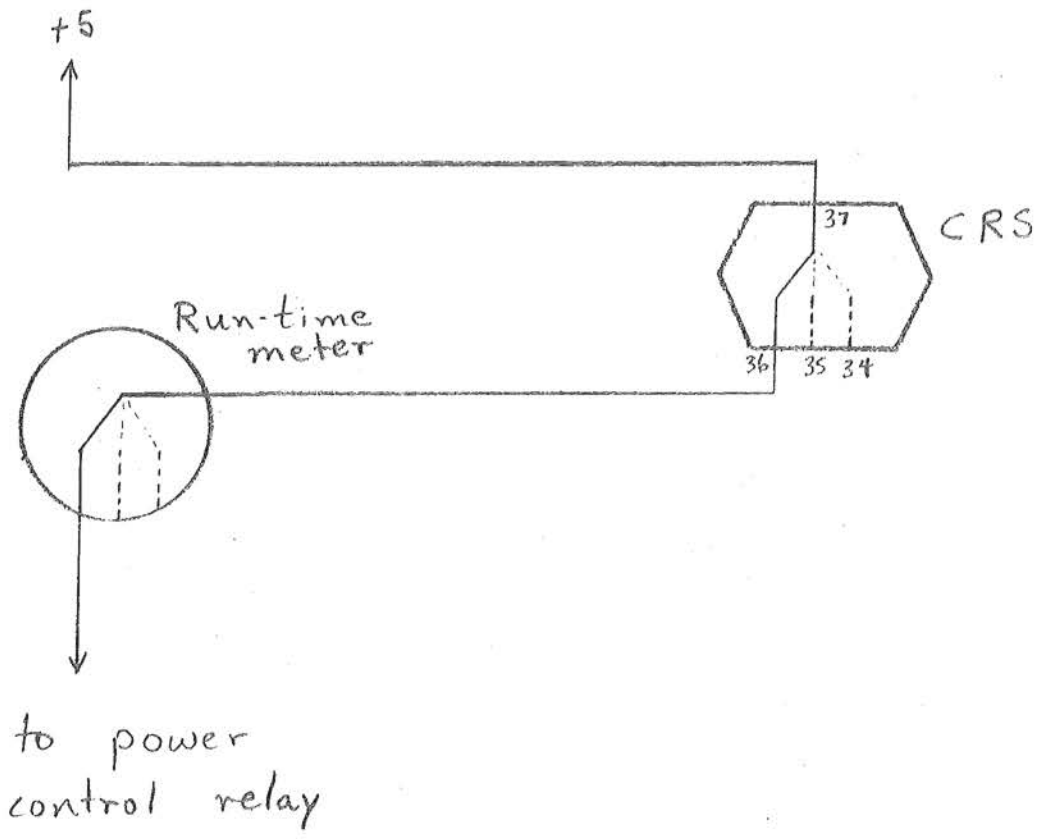


Figure 3b. Keying of run-time meter to instrument. PTM is shown.

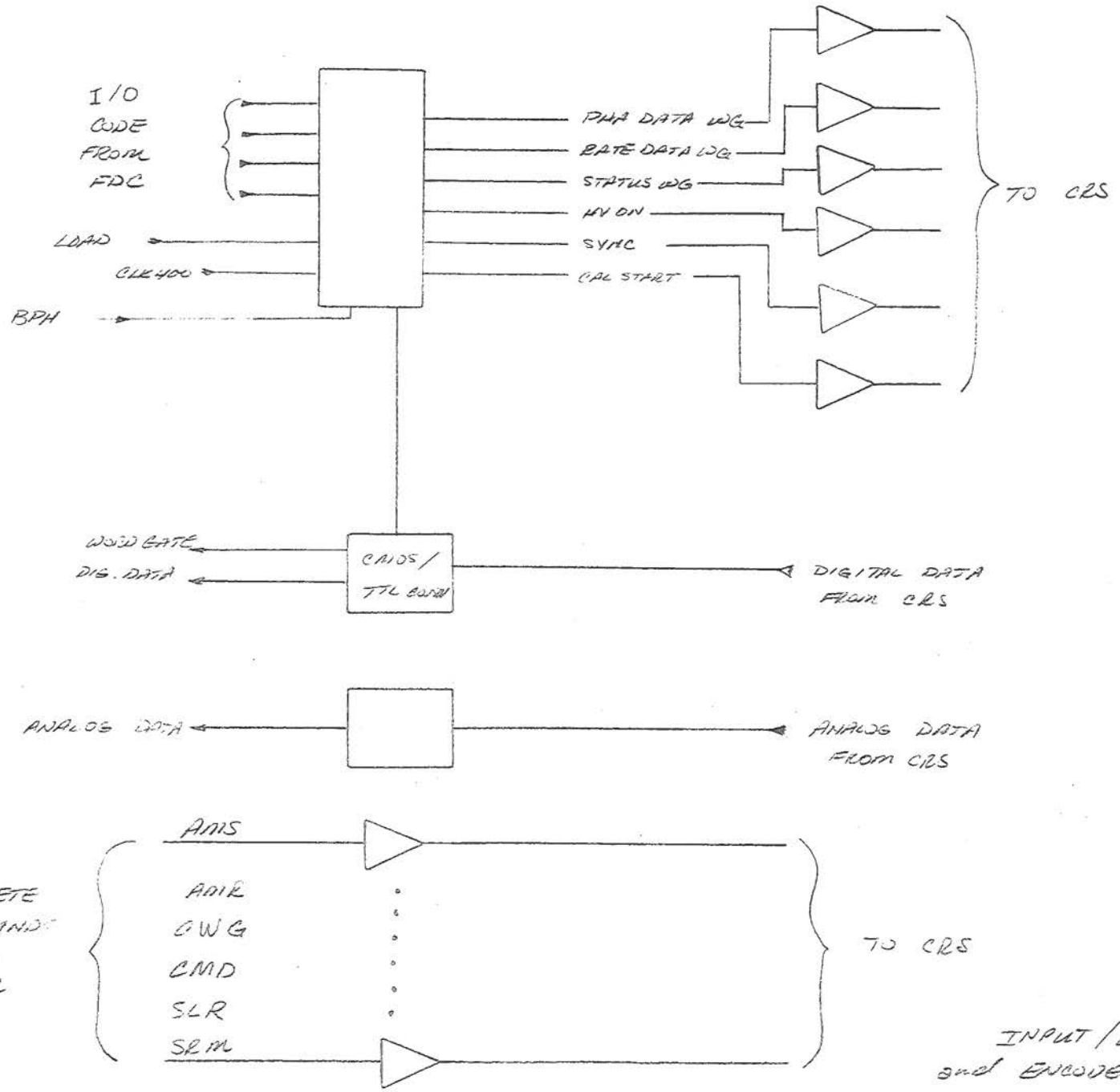
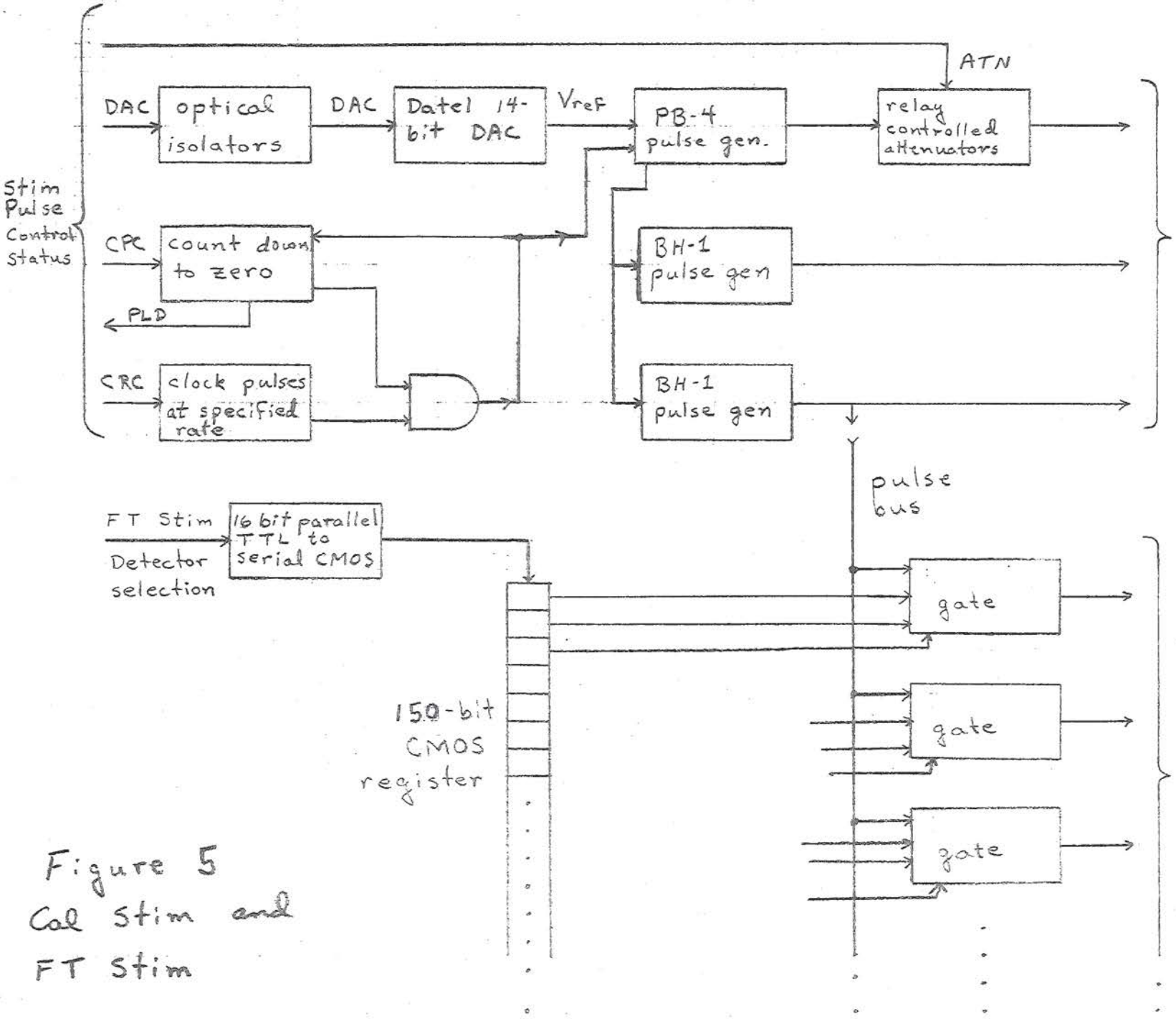


Fig. 4

INPUT/OUTPUT BUFFERS
and ENCODERS

V.4



Either Cal Stim or FT Stim but not both is connected to 50 line coax cable to CRS test inputs.

Figure 5
Cal Stim and FT Stim

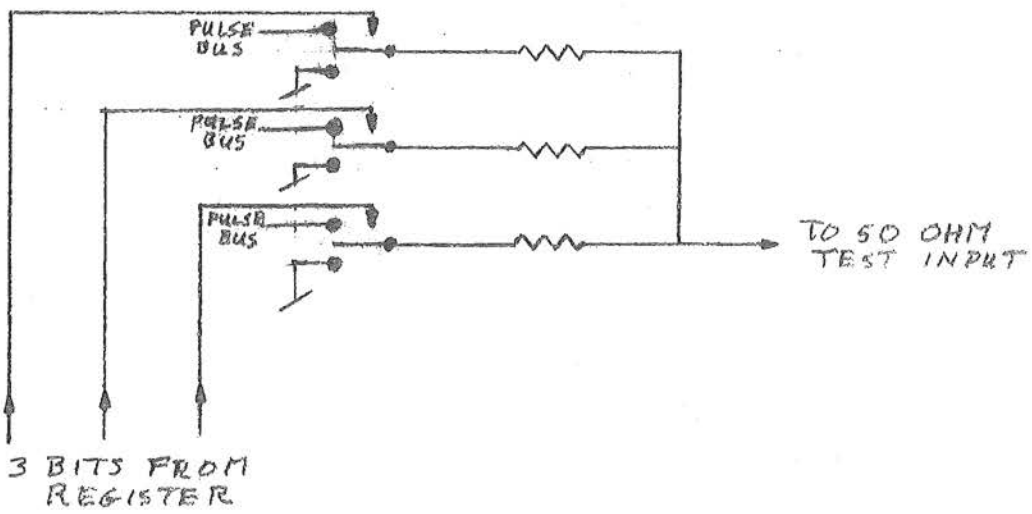
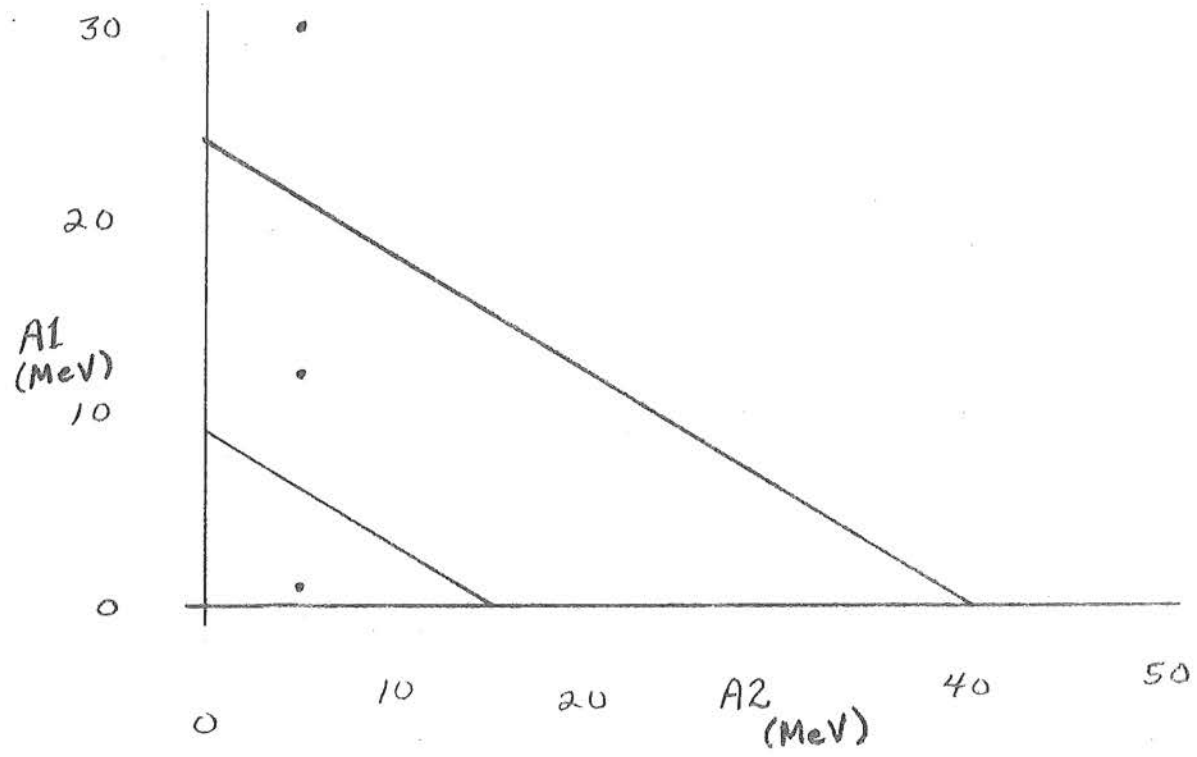
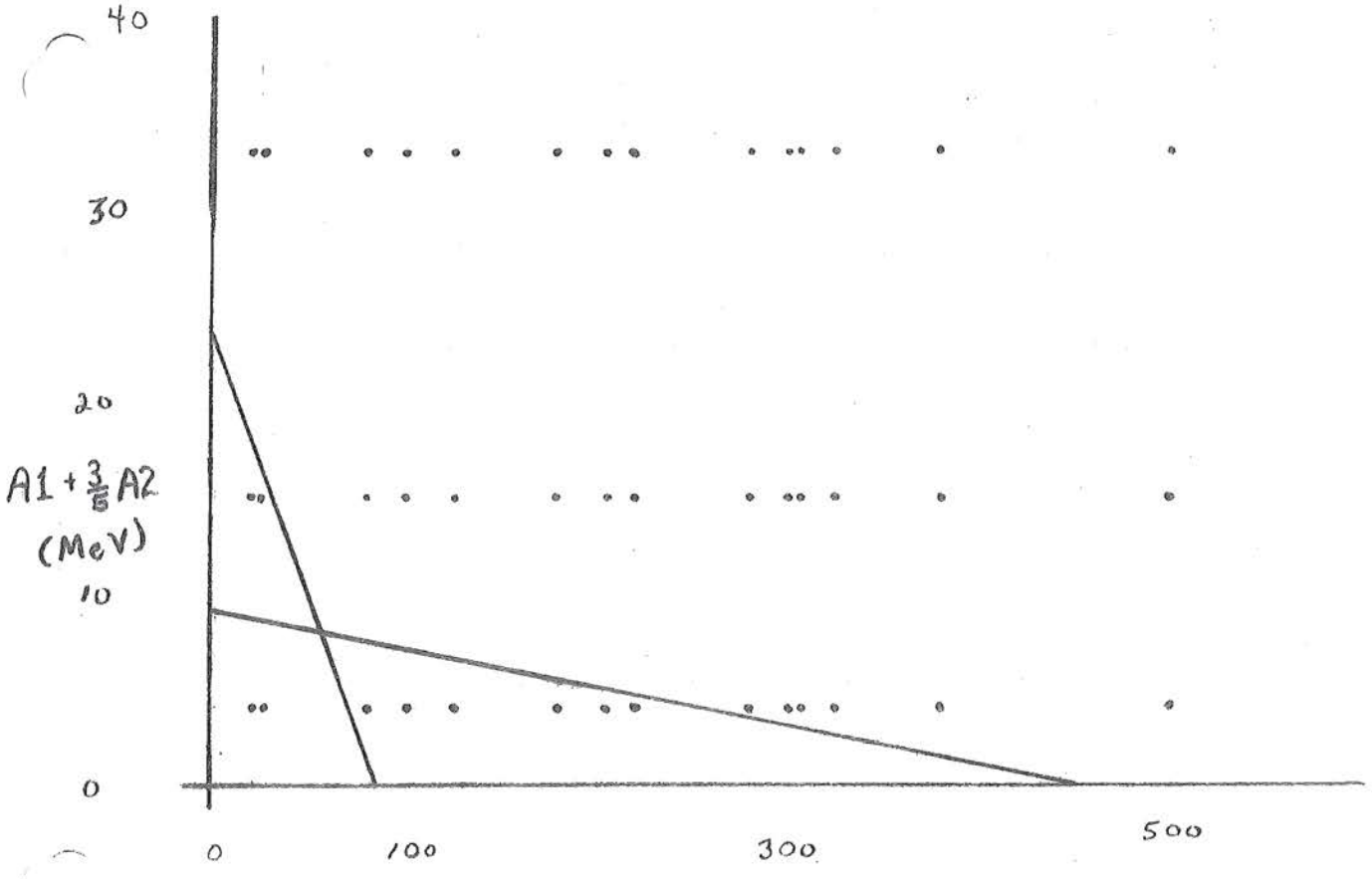


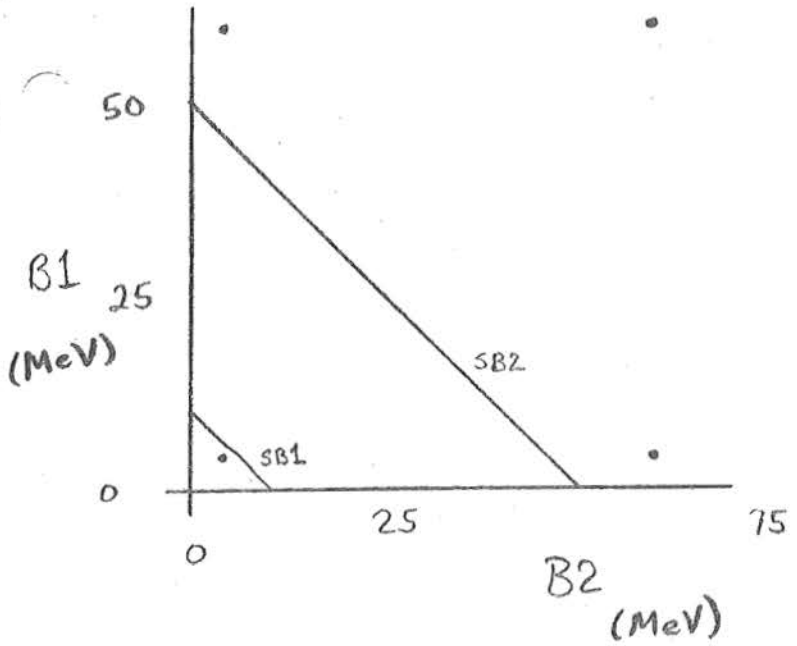
Figure 6. Details of FT Stim gates





C1 + C2 + C3
(MeV)

Fig 7a


50
B1
25
(MeV)
SB2
SB1
0
0
25
75
B2
(MeV)

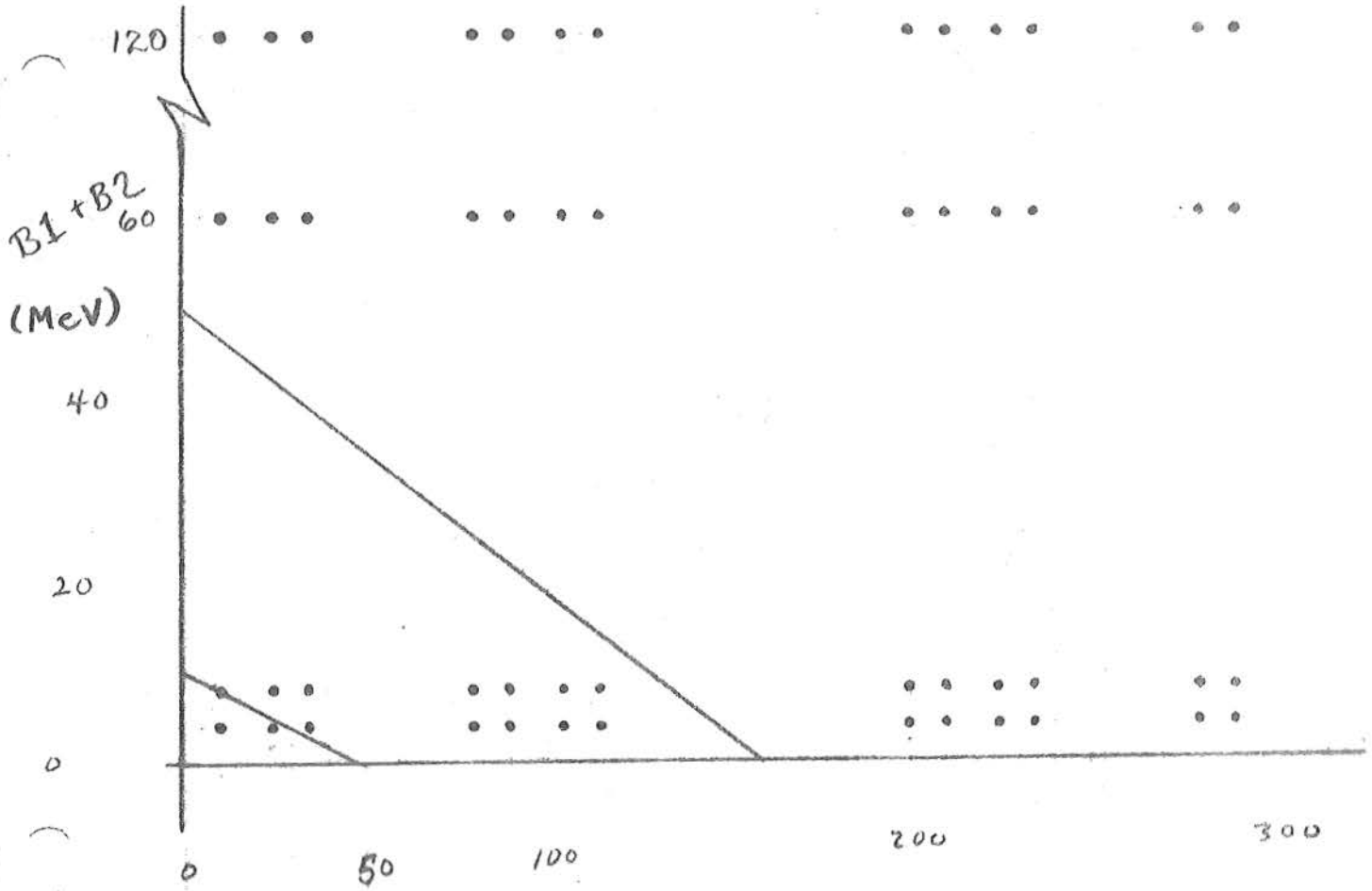

120
B1+B2
60
(MeV)
40
20
0
0
50
100
200
300
C4+C3+C2
(MeV)

Fig 7b

VIII. Tables of Signals

This section lists relevant signals in several formats. Table 1 lists signals in logical groupings and specifies which hardware modules are connected to each. Table 2 is a breakdown of the various word gate modes, set by the WGM signal. Table 3 lists the signals used to specify FT Stim states. Table 4 lists the connections to the DECkits. Table 5 lists signals by alphabetical order of mnemonic or acronym.

The notation used for DECkit connections follows:

> The input registers are numbered ØIR through 71R, the output registers are number ØOR through 7OR. Bits are numbered Ø through 15 with the interrupt line on the input registers labelled as bit 16. Thus the first bit on the second output register is 1ORØ. Numeral zeros are slashed to avoid confusion.

Table 1. SIGNAL LIST

Signals	Mnemonic	ADPE interface
FDS to CRS		
Command Word Gate	CWG	
Command Word	CMD	ØOR⟨Ø:11⟩
Analog Mux Step	AMS	1OR11
Analog Mux Reset	AMR	1OR12
PHA Data Word Gate A	PGA	
PHA Data Word Gate B	PGB	
Rate Data Word Gate A	RGA	
Rate Data Word Gate B	RGB	
Status Word Gate	SWG	
Synch	SNK	
Cal Start	CLS	1OR9
Redundancy Select	SLR	1OR6
HV On	HVN	1OR1Ø
A Phase Clock	APH	AR-11 ext.
B Phase Clock	BPH	clock input
CRS to FDS		
Digital Data A	DGA	DGD = DGA + DGB
Digital Data B	DGB	2IR⟨Ø:11⟩
Analog Data	ADT	AR-11 ADCØ
Analog Signals		
Telescope Thermistor	TTM	AR-11 ADC1
Electronics Thermistor	ETM	ADC2
Room Temp Probe	RTM	ADC3
28V Power-Voltage	VLT	ADC4
28V Power-Current	CRN	ADC5
Cal Stim		
Cal Stim Amplitude	DAC	3OR⟨Ø:14⟩
Attenuator	ATN	4OR⟨Ø:3⟩
Rate Control	CRC	2OR⟨12:13⟩
Pulse Count	CPC	2OR⟨Ø:11⟩
Other		
Power on/off	PWR	1ØR14
PWR Enable	PWE	1ØR13
Analog Mux Status	AMX	ØIR⟨Ø:4⟩
Command Word Flag	CWF	ØIR16
SLR Enable	SLE	1ØR5
Redundancy Select (in)	SLR	1IRØ
Word Gate Mode	WGM	1ØR⟨2:4⟩
WGM Enable	WGE	1ØRØ
Word Gate Continue	WGC	1ØR1
Hardware Clear	HCR	1OR15
Rate Mux Status	RMX	4IR⟨Ø:8⟩
Stop Rate Mux	SRM	1OR8
SRM Enable	SRE	1OR7
Digital Data Code	DGC	1IR⟨1:2⟩
Digital Data Interrupt	DGI	2IR16
PWG Count of 4	PCT	1IR⟨3:4⟩
Pulsing Done	PLD	1IR16

Table 2. Word Gate and Digital Data Codes

WGM	Word Gate Mode	
0	30 Rate	rate acq.
1	SNK·16(30 Rate·Status)	rate or status acq.
2	4 PHA	software mode
3	1 Rate	
4	1 Status	
5.	16 [(BS Status) 30 (Rate 4 PHA)] at 400 Hz	spacecraft normal
6.	" " at 5 Hz	
7.	SNK	

(BS = Blank or Synch)

DGC	Digital Data Code
00	PHA
01	Rate
10	Status

Table 3. FT Stim States

Word	Bit	Preamp	Energy
1	5	H1A1	1
	4		12
	3		30
	2	H1A2	5
	1		0
	0		0
2	15	H1B1	4
	14		60
	13		0
	12	H1B2	4
	11		60
	10		0
	9	H1C1	20
	8		100
	7		200
	6	H1C2	80
	5		200
	4		0
	3	H1C3	24
	2		200
	1		0
	0	H1C4	10
3	15	H1C4	0
	14		0
	13	H1G1	1.5
	12		5
	11		20
	10	H1G2	1.5
	9		0
	8		0
	7	H1G3	1.5
	6		0
	5		0
	4	H1G4	1.5
	3		0
	2		0
	1	H2A1	1
	0		12
4	15	H2A1	30
	14	H2A2	5
	13		0
	12		0
	11	H2B1	4
	10		60
	9		0
	8	H2B2	4
	7		60
	6		0

Table 3 (cont'd.)

Word	Bit	Preamp	Energy
	5	H2C1	20
	4		100
	3		200
	2	H2C2	80
	1		200
	0		0
5	15	H2C3	24
	14		200
	13		0
	12	H2C4	10
	11		0
	10		0
	9	H2G1	1.5
	8		5
	7		20
	6	H2G2	1.5
	5		0
	4		0
	3	H2G3	1.5
	2		0
	1		0
	0	H2G4	1.5
6	15		0
	14		0
	13	LAL1	5
	12		24
	11		0
	10	LAL2	5
	9		24
	8		0
	7	LAL3	5
	6		60
	5		0
	4	LAL4	5
	3		0
	2		0
	1	LBL1	5
	0		24
7	15		0
	14	LBL2	5
	13		24
	12		0
	11	LBL3	5
	10		60
	9		0
	8	LBL4	5
	7		0
	6		0

Word	Bit	Preamp	Energy
	5	LCL1	5
	4		24
	3		0
	2	LCL2	5
	1		24
	0		0
8	15	LCL3	5
	14		60
	13		0
	12	LCL4	5
	11		0
	10		0
	9	LDL1	5
	8		24
	7		0
	6	LDL2	5
	5		24
	4		0
	3	LDL3	5
	2		60
	1		0
	0	LDL4	5
9	15		0
	14		0
	13	D1	1
	12		10
	11		0
	10	D2	1
	9		10
	8		0
	7	D3	1
	6		15
	5		0
	4	D4	1
	3		15
	2		0
	1	D5	1
	0		15
10	15		0
	14	D6	1
	13		15
	12		0
	11	D7	1
	10		15
	9		0

Table 3 (cont'd.)

Word	Bit	Preamp	Energy
	8	D8	1
	7		0
	6		0
	5	GA	1
	4		0
	3		0
	2	GB	1
	1		0
	0		0

Table 4. ADPE Registers

	Register	Bits	Use	
Input:	ØIR	<Ø:4>	AMX	
		<5:15>	(unused)	
		16	CWF	
	1IR	Ø	SLR	
		<1:2>	DGC	
		<3:4>	PCT	
		<5:13>	RMX	
		<14:15>	(unused)	
		16	PLD	
	2IR	<Ø:11>	DC = DGA + DGB	
		<12:15>	(unused)	
		16	DGI	
	3IR		(unused)	
	4IR		(unused)	
	5IR		(unused)	
	6IR		(unused)	
	7IR		(unused)	
Output:	ØOR	<Ø:11>	CMD	
		<12:15>	(unused)	
	1OR	Ø	WGE	
		1	WGC	
		<2:4>	WGM	
		5	SLE	
		6	SLR	
		7	SRE	
		8	SRM	
		9	CLS	
		10	HVN	
		11	AMS	
		12	AMR	
		13	PWE	
		14	PWR	
		15	HCR	
	2OR	<12:13>	CRC	Cal Stim
		<Ø:11>	CPC	
	3OR	<Ø:14>	DAC	
	4OR	<Ø:3>	ATN	
	5OR	<Ø:15>	FT Stim	
	6OR		(unused)	
	7OR		(unused)	

TABLE 5 ALPHABETICAL LIST OF SIGNAL MNEMONICS

NAME	SIGNAL	COMMENTS
ADT	Analog Data	from CRS
AMR	Analog Mux Reset	to CRS
AMS	Analog Mux Step	to CRS
AMX	Analog Mux Status	FDC register for ADPE to read
APH	A Phase Clock	
ATN	Cal Stim Attenuator	
BPH	B Phase Clock	
CLS	Cal Start	to CRS
CMD	Command	to CRS
CPC	Cal Stim Pulse Count	no of pulses to be output
CRC	Cal Stim Rate Control	rate of pulsing
CRN	Current	current on 30V line to CRS
CWF	Command Word Flag	means command was issued
CWG	Command Word Gate	to CRS
DAC	Cal Stim Pulse Amplitude	
DGA	Digital Data A	from CRS
DGB	Digital Data B	from CRS
DGC	Digital Date Code	see table 2
DGD	Digital Data	DGA + DGB
DGI	Digital Data Interrupt	Says data is available
ETM	Electronics Temperature	from CRS
HCR	Hardware Clear	Clears registers in digital control-status, etc.
HVN	High Voltage On	to CRS. Must be switch enabled.
PCT	PWG Count of 4	
PLD	Pulsing Done	from Stim to ADPE
PWE	PWR Enable	gates PWR from ADPE to relay
PWR	Power On/Off	Requires PWE and switch enable
RMX	Rate Mux Status	FDC register for ADPE to read
RTM	Room Temperature	
SLE	SLR Enable	
SLR	Redundancy Select	to CRS
SNK	Synch	to CRS
SRE	SRM Enable	
SRM	Stop Rate Mux	

TABLE 5 cont'd

TTM	Telescope Temperature	from CRS
VLT	Voltage	on 30V line to CRS
WGC	Word Gate Continue	repeat word gate pattern
WGE	WGM Enable	
WGM	Word Gate Mode	specifies which pattern. See Table 2.