SAM-1-O-08106 Rev C

COMMAND DESCRIPTION

FOR THE

SAMPEX DATA PROCESSING UNIT (DPU)

NASA COOPERATIVE AGREEMENT #26979B

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HILT INTERNAL STIMULATION - DAC IK & PC (HDACIKPC):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=1	=81 HEX	DAC IK	DAC PC	=0	=0	CHECKSUM

HILT INTERNAL STIMULATION - DAC CSJ & SSD (HDACCSSS):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=2	=82 HEX	DAC CSI	DAC SSD	=0	=0	CHECKSUM

HILT INTERNAL STIMULATION - DELAY & CHOPPER ENABLE (HDELCHOP):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=3	=83 HEX	CONTROLWORD		=0	=0	CHECKSUM

CONTROLWORD BIT DEFINITION:
15 - SELECT INTERNAL CHOPPER (0 = EXTERNAL CHOPPER)
14:12 - DELAY SETTING
11 - ENABLE CHOPPER IKE
10 - ENABLE CHOPPER PCE
9 - ENABLE CHOPPER PC-POS
5 - ENABLE CHOPPER SSDT1 (SPARE)
4 - ENABLE CHOPPER CSI
3 - ENABLE CHOPPER SSD4
2 - ENABLE CHOPPER SSD3
1 - ENABLE CHOPPER SSD2
0 - ENABLE CHOPPER SSD1

HILT TIME CODE (HTIME):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=4	=84 HEX	TIMECODE		=0	=0	CHECKSUM

TIMECODE DEFINITION:
- 15 - HOURS (LSB)
- 14:12 - TENS OF MINUTES (BCD FORMAT)
- 11:8 - ONES OF MINUTES (BCD FORMAT)
- 7:4 - TENS OF SECONDS (BCD FORMAT)
- 3:0 - ONES OF SECONDS (BCD FORMAT)

HILT ENABLE SSD ROWS (HENROWS):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=5	=85 HEX	CONTROLWORD		=0	=0	CHECKSUM

CONTROLWORD DEFINITION:
- 15:13 - NO STORAGE
- 12 - HIGH ENERGY MODE ON (SUBSTITUTE PC, IK, TOD IN LOGIC)
- 11 - INTERNAL STIMULATION ON
- 10 - SUBCOM A2
- 9 - SUBCOM A1
- 8 - SUBCOM A0
- 7 - DISABLE CSI 4
- 6 - DISABLE CSI 3
- 5 - DISABLE CSI 2
- 4 - DISABLE CSI 1
- 3 - ENABLE SSD ROW 4
- 2 - ENABLE SSD ROW 3
- 1 - ENABLE SSD ROW 2
- 0 - ENABLE SSD ROW 1

HILT ENABLE EVENTS (HENEVTS):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=6	=86 HEX	CONTROLWORD		=0	=0	CHECKSUM

CONTROLWORD DEFINITION: 15:8 - NO STORAGE
3 - ENABLE EVENT HE1
2 - ENABLE EVENT HE2
1 - ENABLE EVENT HZ1
0 - ENABLE EVENT HZ2

HILT SET EEPROM ADDRESS (HEEPADDR):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=7	=87 HEX	EEPROM ADDRESS		=0	=0	CHECKSUM

HILT XILINX CONTROL (HXICNTL):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=11 HEX	=8	=88 HEX	CONTROL	DATA	=0	=0	CHECKSUM

CONTROL DEFINITION: 4 - LCA UNIT SELECT
3 - WRITE EEPROM
2 - LCA READBACK MODE
1 - LCA MASKED MODE
0 - LCA COMPARE MODE

LEICA TIME CODE (LTIME):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=22 HEX	=1	=A0 HEX	TIMECODE		=0	=0	CHECKSUM

TIMECODE DEFINITION: 15 - HOURS (LSB)
14:12 - TENS OF MINUTES (BCD FORMAT)
11:8 - ONES OF MINUTES (BCD FORMAT)
7:4 - TENS OF SECONDS (BCD FORMAT)
3:0 - ONES OF SECONDS (BCD FORMAT)

LEICA SUBCOM STATE (LSUBCOM):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=22 HEX	=2	=A2 HEX	=0	SUBCOM	=0	=0	CHECKSUM

LEICA SENSOR CONTROL (LCONTROL):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=22 HEX	=3	=A4 HEX	CONTROLWORD		=0	=0	CHECKSUM

CONTROLWORD DEFINITION: 15:14 - PROTON SLANT SLOPE SELECTION
13:7 - PROTON SLANT THRESHOLD
6 - IN FLIGHT CALIBRATOR ENABLE, 1=ENABLE (IFC ON), 0=DISABLE (IFC OFF)
5 - STOP SEDA HVPS ENABLE, 1=ENABLE, 0=DISABLE
4 - START SEDA HVPS ENABLE, 1=ENABLE, 0=DISABLE
3 - SSD4 ENABLE, 1=ENABLE, 0=DISABLE
2 - SSD3 ENABLE, 1=ENABLE, 0=DISABLE
1 - SSD2ENABLE, 1=ENABLE, 0=DISABLE
0 - SSD1 ENABLE, 1=ENABLE, 0=DISABLE

LEICA HIGH VOLTAGE, HV1 (LHIGHVL1)

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=22 HEX	=4	=A6 HEX	=0	LEVEL	=0	=0	CHECKSUM

LEICA HIGH VOLTAGE, HV2 (LHIGHVL2)

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=22 HEX	=5	=A7 HEX	=0	LEVEL	=0	=0	CHECKSUM

MAST CONTROLWORD (MCNTRL):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=33 HEX	=1	=C7 HEX	=0	SUBCOM COUNTER		CONTROL	CHECKSUM

CONTROL DEFINITION: 7:4 - SECTOR COUNTER
3:0 - HK MUX ADDRESS

MAST COMMAND WORD 1 (MCMDWRD1):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=33 HEX	=2	=C1 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:

31 - /D1/	15 - /G2L*/
30 - /D1S/	14 - [G2P*]
29 - [D1]	13 - [H]
28 - [D2]	12 - [HAZ*]
27 - [D3]	11 - [KH0]
26 - [D4]	10 - [KH1]
25 - [D5]	9 - [KH2]
24 - [D6]	8 - [KH3]
23 - [D7*]	7 - [KH4]
22 - /D6/	6 - [KH5]
21 - /D6*/	5 - [KH6]
20 - [D7P]	4 - [KP]
19 - /G1H*/	3 - CAL OFF
18 - [G1L*]	2 - CMND CAL TRIG
17 - /G1P*/	1 - ACE EN
16 - [G2H*]	0 - NDW-A

MAST COMMAND WORD 2 (MCMDWRD2):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=33 HEX	=3	=C2 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:

31	[KZ10]	15	/M1X1/
30	[KZ11]	14	[M1XS]
29	[KZ12]	13	/M2Y1/
28	[KZ13]	12	[M2YS]
27	[KZ14]	11	/M1X/
26	[KZ15]	10	/M2Y/
25	[KZ16]	9	/M1XM2Y/
24	[KZ20]	8	/M3X1/
23	[KZ21]	7	[M3XS]
22	[KZ22]	6	/M4Y1/
21	[KZ23]	5	[M4YS]
20	[KZ24]	4	/M3X/
19	[KZ25]	3	/M4Y/
18	[KZ26]	2	/M3XM4Y/
17	/L/	1	/Z1SECZ2/
16	[L*]	0	NDW-B

MAST COMMAND WORD 3 (MCMDWRD3):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=33 HEX	=4	=C3 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:
31:28 - M4YSB
27:24 - M4YSA
23:20 - M3XSB
19:16 - M3XSA
15:12 - M2YSB
11:8 - M2YSA
7:4 - M1XSB
3:0 - M1XSA

MAST COMMAND WORD 4 (MCMDWRD4):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=33 HEX	=5	=C4 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:
31:28 - D4B
27:24 - D4A
23:20 - D3B
19:16 - D3A
15:12 - D2B
11:8 - D2A
7:4 - D1B
3:0 - D1A

MAST COMMAND WORD 5 (MCMDWRD5):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=33 HEX	=6	=C5 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:
22 - D7 D EN
21 - G6 HD EN
20 - G6 LD EN
19 - G47 HD EN
18 - G47 LD EN
17 - G35 HD EN
16 - G35 LD EN
15:12 - D6B
11:8 - D6A
7:4 - D5B
3:0 - D5A

MAST COMMAND WORD 6 (MCMDWRD6):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=33 HEX	=7	=C6 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:

20 - LVTMDIS
19 - D6 ADC EN
18 - D5 ADC EN
17 - D4 ADC EN
16 - D3 ADC EN
15 - D2 ADC EN
14 - D1 ADC EN
13 - M4YS ADC EN
12 - M4Y1 ADC EN
11 - M3XS ADC EN
10 - M3X1 ADC EN
9 - M2YS ADC EN
8 - M2Y1 ADC EN
7 - M1XS ADC EN
6 - M1X1 ADC EN
5 - ADC CAL EN
4 - RMP CAL EN
3 - LOG CAL EN
2 - [Z3*]
1 - /Z3B/
0 - [Z3A]

PET CONTROLWORD (PCNTRL):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=44 HEX	=1	=A7 HEX	=0	SUBCOM COUNTER		CONTROL	CHECKSUM

CONTROL DEFINITION: 7:4 - SECTOR COUNTER
3:0 - HK MUX ADDRESS

PET COMMAND WORD 1 (PCMDWRD1):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=44 HEX	=2	=A1 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:
28 - P4 D EN
27 - P5 D EN
26 - P6 D EN
25 - P7 D EN
24 - P8 D EN
23 - A3 LD EN
22 - A3 HD EN
21 - A4 LD EN
20 - A4 HD EN
19 - A57 LD EN
18 - A57 HD EN
17 - A68 LD EN
16 - A68 HD EN
15:12 - P3B
11:8 - P3A
7:4 - P1B
3:0 - P1A

PET COMMAND WORD 2 (PCMDWRD2):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=44 HEX	=3	=A2 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:

31 - [P1]
30 - [P1*]
29 - [P1A]
28 - [P1A*]
27 - [P2]
26 - /P2*/,[P2E]
25 - [P3]
24 - [P3*]
23 - /P3*/
22 - /P3A/
21 - /P3E/
20 - /P3P/
19 - /P3AE/
18 - [P3B*]
17 - [P4]
16 - [P4*]
15 - /P4/
14 - /P5/
13 - /P5*/
12 - /P7/
11 - /P7*/
10 - [P8]
9 - [P8*],[P8R*]
8 - [AL*]
7 - [ALE*]
6 - [ALR*]
5 - /ALP*/
4 - /AH*/
3 - /AHE*/
2 - /AHR*/
1 - /AHP*/
0 - NDW-A

PET COMMAND WORD 4 (PCMDWRD4):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=44 HEX	=4	=A4 HEX	CONTROL LONGWORD				CHECKSUM

CONTROL LONGWORD DEFINITION:

23 - [RP]
22 - [RE]
21 - [RR]
20 - [REW]
19 - [RPN]
18 - P1 ADC EN
17 - P2 ADC EN
16 - P3 ADC EN
15 - P47 ADC EN
14 - HIZ EN
13 - LOZ EN
12 - LOG CAL DIS
11 - RMP CAL DIS
10 - ADC CAL DIS
9 - CMND CAL TRIG
8 - ACE EN
7 - [HAZ*]
2 - LVTMDIS
1 - CALIBRATE OFF
0 - NDW-B

SEDS TIME DISTRIBUTION (SEDSTIME):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=1	DAYS SINCE 24-MAY-68		SECONDS OF DAY			CHECKSUM

SEDS MEMORY STATUS (SEDSMEM): **DELETED**

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=2	TOTAL MEMORY AVAILABLE FOR SCIENCE (IN BYTES)				=0	CHECKSUM

SYSTEM RESET (RESET):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=3	=0	=0	=0	=0	=0	CHECKSUM

READ DPU MEMORY BLOCK (READDPU):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=4	STARTING ADDRESS		=0	=0	=0	CHECKSUM

SET DPU MEMORY MODIFICATION STARTING ADDRESS FOR WRITE (SETDADDR):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=5	STARTING ADDRESS		=0	=0	=0	CHECKSUM

OVERWRITE DPU MEMORY (WRITEDPU):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=6	LENGTH	DATA1	DATA2	DATA3	DATA4	CHECKSUM

LENGTH = 0, 1, 2, 3, or 4 and indicates the number of DATA bytes which follow.

START OF GROUND PASS (STRTPASS):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=7	=0	=0	=0	=0	=0	CHECKSUM

END OF GROUND PASS (ENDPASS):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=8	=0	=0	=0	=0	=0	CHECKSUM

END OF CONFIGURATION COMMAND LIST (ENDLIST):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=9	=0	=0	=0	=0	=0	CHECKSUM

ENABLE ASYNCHRONOUS DATA SOURCES (ENABDATA):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=10	ITEMMASK	NEWSTATE	=0	=0	=0	CHECKSUM

ITEMMASK BITS: 7=HILT EVENTS, 6=LEICA EVENTS, 5=MAST EVENTS, 4=PET EVENTS, 3=HILT HRR, 2=PET HRR
NEWSTATE VALUES: 1=ON, 2=OFF

MAST/PET LVPS CONTROL (LVPSCNTL):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=11	ITEMMASK	NEWSTATE	=0	=0	=0	CHECKSUM

ITEMMASK BITS: 7=OSC, 6=MAST POWER, 5=PET POWER
NEWSTATE VALUES: 1=ENABLE, 2=DISABLE

HILT VALVE AND COVER CONTROL (HILTVALV):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=12	ITEMMASK	NEWSTATE	TIMEOUT(SECS)		=0	CHECKSUM

ITEMMASK BITS: 7=MAIN VALVE, 6=VENT VALVE, 5=FLOW REGULATION, 4=GAS REGULATION, 3=COVER
NEWSTATE VALUES: 1=OPEN, 2=CLOSE (FOR GAS REGULATION 1=ON, 2=OFF)

HILT HIGH-VOLTAGE ENABLE (HILTHVEN):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=13	ITEMMASK	NEWSTATE	SSDITEM	PCFE THRS.	SSD THRS.	CHECKSUM

ITEMMASK BITS: 7=SSD, 6=DRIFT, 5=PC
NEWSTATE VALUES: 1=ENABLE, 2=DISABLE

SSDITEM = 1,2,3, OR 4
REAL THRESHOLDS ARE 2^PCFE THRS. AND 2^SSD THRS.

READ EEPROM/LCA MEMORY (READHILT):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=14	MASK	STARTING ADDRESS		LENGTH		CHECKSUM

MASK BITS: 4=LCA UNIT SELECT, 3=UNUSED, 2=LCA READBACK, 1=LCA MASKED, 0=LCA COMPARE
STARTING ADDRESS & LENGTH FIELDS MUST BOTH BE MULTIPLES OF 8

SET EEPROM/LCA STARTING ADDRESS FOR WRITE (SETHADDR):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=15	STARTING ADDRESS		=0	=0	=0	CHECKSUM

WRITE EEPROM/LCA DATA (WRITHILT):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=16	DATA1	DATA2	DATA3	DATA4	BLKCTRL	CHECKSUM

BLKCTRL MEANING: 0=END OF BLOCK WRITE, 1=NOT THE END OF BLOCK

HILT/LEICA EVENT MEMORY ALLOCATION PER ORBIT (HLORBIT):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=17	HILT ALLOCATION / 256		LEICA ALLOCATION / 256		=0	CHECKSUM

MAST/PET EVENT MEMORY ALLOCATION PER ORBIT (MPORBIT):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=18	MAST ALLOCATION / 256		PET ALLOCATION / 256		=0	CHECKSUM

HIGH-RESOLUTION RATE ALLOCATION PER ORBIT (HRRORBIT):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=19	HILT HRR ALLOC. / 256		PET HRR ALLOC. / 256		=0	CHECKSUM

SET REALLOCATION PERCENTAGES - HILT, LEICA, MAST EVENTS (REALLOC1):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=20	HILT EVT	LEICA EVT	MAST EVT	=0	=0	CHECKSUM

ALL REALLOCATION NUMBERS REFER TO N/32 OF TOTAL UNUSED MEMORY

SET REALLOCATION PERCENTAGES - PET EVENTS, HILT & PET HIGH-RES RATES (REALLOC2):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=21	PET EVT	HILT HRR	PET HRR	=0	=0	CHECKSUM

ALL REALLOCATION NUMBERS REFER TO N/32 OF TOTAL UNUSED MEMORY

HILT 1 SECOND EVENT QUOTAS (HILT1SEC):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=22	HE1 QUOTA	HE2 QUOTA	HZ1 QUOTA	HZ2 QUOTA	=0	CHECKSUM

LEICA 1 SECOND EVENT QUOTAS (LEIC1SEC):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=23	HI+LO PRI	LO-PRI	=0	=0	=0	CHECKSUM

MAST 1 SECOND EVENT QUOTAS (MAST1SEC):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=24	HIZ-QUOTA	PEN-QUOTA	Z2-QUOTA	Z1-QUOTA	HAZ-QUOTA	CHECKSUM

PET 1 SECOND EVENT QUOTA (PET1SEC):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=25	1 SEC QUOTA	=0	=0	=0	=0	CHECKSUM

ENABLE INTERFACES (ENABINTS):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=26	ITEMMASK	NEWSTATE	=0	=0	=0	CHECKSUM

ITEMMASK BITS: 7=HILT, 6=LEICA, 5=MAST, 4=PET
NEWSTATE VALUES: 1=ENABLE, 2=DISABLE

PET HIGH-RES RATE THRESHOLD (PETTHRES):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=27	THRESHOLD		=0	=0	=0	CHECKSUM

HILT HIGH-RES RATE THRESHOLD (HLTTHRES):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=28	ITEM #	THRESHOLD		=0	=0	CHECKSUM

ITEM # SPECIFIES PARAM TO CHECK AGAINST THRESHOLD: 1=SSD1, 2=SSD2, 3=SSD3, 4=SSD4, 5=IK, 6=PCRE

START HISTORY DATA READOUT (STRTHIST):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=29	MASK	=0	=0	=0	=0	CHECKSUM

MASK BITS: 7=HILT ENABLE, 6=LEICA ENABLE, 5=MAST ENABLE, 4=PET ENABLE, 3=DPU ENABLE

DUMP DPU PARAMETER AREA (PARAMDMP):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=30	=0	=0	=0	=0	=0	CHECKSUM

RESET DPU COMMAND COUNTERS (RSTCNTRS):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=31	=0	=0	=0	=0	=0	CHECKSUM

RESTART MEMORY QUOTAS (RSTQUOTA):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=32	=0	=0	=0	=0	=0	CHECKSUM

HILT POWER RELAY (HILTRLY):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=33	NEWSTATE	=0	=0	=0	=0	CHECKSUM

NEWSTATE VALUES: 1=ON, 2=OFF

XILINX CONTROL (XICONTRL):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=34	XMASK	WORDADDR	PARAMETER		=0	CHECKSUM

XMASK BITS: 7=OVERRIDE XINIT/XPWROFF ALGORITHM, 6=SEND XINIT, 5=SEND XPWROFF, 1:0=OPCODE (BELOW)
OPCODE SETTINGS: 3=NOP, 2=SEND SINGLE HILT CMD, 1=READ HILT DATAWORD, 0=NOP
PARAMETER: =CMD CODE (IF OPCODE = 2), =# OF READOUTS (IF OPCODE = 1) MAXIMUM = 32

ANALOG CONTROL (ANCONTRL):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=35	AOSC	=0	=0	=0	=0	CHECKSUM

AOSC INDICATES THE OSCILLATOR TO USE (0 OR 1)

DPU CONFIGURATION CONTROL (DPUCONF):

BYTE 0	BYTE 1	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6	BYTE 7
=55 HEX	=36	CTLMASK	CTLSEL	=0	=0	=0	CHECKSUM

CTLMASK BITS: 1=ENABLE CHECKING OF MISCELLANEOUS GATE ARRAY BIT
0=ENABLE CHECKING OF CPU CONTROL GATE ARRAY BIT

CTLSEL BITS: 1=DESIRED MISCELLANEOUS GATE NUMBER
0=DESIRED CPU CONTROL GATE ARRAY NUMBER

ACTION: IF CURRENT DPU STATUS DOES NOT INDICATE THAT SPECIFIED CPU CONTROL AND MISCELLANEOUS GATE ARE IN USE, THEN REBOOT WILL OCCUR. THIS COMMAND WILL ONLY BE USED IN THE BOOT LIST IN CASE SOMETHING GOES WRONG WITH ONE OF THE REDUNDANT GATE ARRAYS; REBOOTING CAUSES GATE ARRAY SWAP.

I. HILT Commands

1) HDACIKPC - HILT Internal Stimulation, DAC IK & PC. This command is simply passed-thru by the DPU. It is used for internal calibration of the HILT instrument and details should be gotten from Berndt Klecker.

2) HDACCSS - HILT Internal Stimulation, DAC CSJ & SSD. This command is simply passed-thru by the DPU. It is used for internal calibration of the HILT instrument and details should be gotten from Berndt Klecker.

3) HDELCHOP - HILT Internal Stimulation, Delay & Chopper Enable. This command is simply passed-thru by the DPU. It is used for internal calibration of the HILT instrument and details should be gotten from Berndt Klecker.

4) HTIME - HILT Time Code. This command is never sent as a ground command to the DPU. It is generated by the DPU, and sent from the DPU to the instrument, as needed to properly operate the HILT instrument.

5) HENROWS - HILT Enable SSD Rows. This command is simply passed-thru by the DPU with the exception of the Subcom which the DPU sets. When the command is received by the DPU, it stores the command in DPU memory so that the next time the Subcom address is changed, it can be done while not changing any of the ground-programmed parameter of this command.

6) HENEVTS - HILT Enable Events. This command is generated in the DPU as necessary to acquire HILT events. It is generated by the DPU only and never requires that a ground command be transmitted.

7) HEEPADDR - HILT Set EEPROM Address. This command is generated in the DPU as necessary to read or write HILT EEPROM/LCA data. It is generated by the DPU only and never requires that a ground command be transmitted.

8) HXICNTL - HILT XILINX Control. This command is generated in the DPU as necessary to read or write HILT EEPROM/LCA data. It is generated by the DPU only and never requires that a ground command be transmitted.

II. LEICA Commands

1) LTIME - LEICA Time Code. This command is never sent as a ground command to the DPU. It is generated by the DPU, and sent from the DPU to the instrument, as needed to properly operate the LEICA instrument.

2) LSUBCOM - LEICA Subcom State. This command is sent from the DPU as

necessary to facilitate readout of the LEICA subcommed analog data. It is generated by the DPU and never requires transmission from the ground.

3) LCONTROL - LEICA Sensor Control. This command is simply passed-thru by the DPU. It is used to change the internal state of the LEICA sensor and details should be gotten from Peter Walpole.

4) LHIGHVL1 - LEICA High Voltage, HV1. This command sets the high-voltage level for high-voltage converter #1. If is simply passed-thru by the DPU. Details on the operation of this command should be supplied by Peter Walpole.

5) LHIGHVL2 - LEICA High Voltage, HV2. This command sets the high-voltage level for high-voltage converter #2. If is simply passed-thru by the DPU. Details on the operation of this command should be supplied by Peter Walpole.

III. MAST Commands

1) MCNTRL - MAST Controlword. This command is generated within the DPU to facilitate the readout of the MAST data. It should never be sent as a ground command to the DPU.

2) MCMDWRD1 - MAST Commandword 1. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

3) MCMDWRD2 - MAST Commandword 2. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

4) MCMDWRD3 - MAST Commandword 3. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

5) MCMDWRD4 - MAST Commandword 4. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

6) MCMDWRD5 - MAST Commandword 5. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

7) MCMDWRD6 - MAST Commandword 6. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

IV. PET Commands

1) PCNTRL - PET Controlword. This command is generated within the DPU to facilitate the readout of the PET data. It should never be sent as a ground command to the DPU.

2) PCMDWRD1 - PET Commandword 1. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

3) PCMDWRD2 - PET Commandword 2. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

4) PCMDWRD4 - PET Commandword 4. This command sets the internal state for the MAST configuration circuitry and comes from the ground only. Details on the operation of this command should be supplied by Alan Cummings.

V. DPU Commands

1) SEDSTIME - SEDS Time Distribution. This command is generated on-board by the SEDS and distributed to the DPU each second to correct any deviation in the DPU's clock for timetagging of packets. This command will never be sent as ground command to the DPU.

2) SEDSMEM - SEDS Memory Status. Deleted.

3) RESET - DPU System Reset. This command causes the DPU to execute it's power-up sequence so that a fresh version of the DPU program can be installed. This command would be needed only in instances where the DPU is not sending telemetry packets at the expected rate which might indicate a problem on board. Proper execution of this command requires that the DPU's command interface is operational, but if not, then the non-essential bus must be powered off to reset the DPU.

4) READDPU - Read DPU Memory Block. Reception of this command by the DPU will result in the transmission of one DPU Memory Dump packet containing a 256-byte block of DPU memory. The packet response will occur within 1 second of the time the command is received by the DPU. The DPU will flag, as errors, any additional READDPU commands until processing of the first received READDPU command is complete.

5) SETDADDR - Set DPU Memory Modification Starting Address for Write. This command is sent prior to the WRITEDPU command to set the address of the first

memory location which will be modified when the WRITEDPU command is sent. For details, see the example given in the WRITEDPU command below.

6) WRITEDPU - Overwrite DPU Memory. This command replaces DPU memory with up to 4 bytes of data found within the command. If we desire to overwrite 11 bytes (overwrite data is 11, 22, ..., BB for this example) of DPU memory starting at location 100, the following sequence of commands would be sent:

6a) SETDADDR, starting address=100.

6b) WRITEDPU, length=4, data1=11, data2=22, data3=33, data4=44

6c) WRITEDPU, length=4, data1=55, data2=66, data3=77, data4=88

6d) WRITEDPU, length=3, data1=99, data2=AA, data3=BB

Notice that the overwrite pointer is automatically incremented by the length field specified in the WRITEDPU command, and therefore the SETDADDR address does not need to be resent after each WRITEDPU command.

7) STRTPASS - Start of Ground Pass. This command is sent to the DPU to enable its output of VC0 real-time telemetry packets. Real-time packets are not output by the DPU unless it believes that a ground pass is currently underway.

8) ENDPASS - End of Ground Pass. This command is sent to the DPU to disable its output of VC0 real-time telemetry packets. If ground contact is not currently established, then real-time DPU packets received by the SEDS cannot be transmitted and so are lost. This command, and the STRTPASS command, are designed to suppress the real-time telemetry packets whenever the ground contact is not enabled.

9) ENDLIST - End of Configuration Command List. The SEDS maintains a DPU configuration command list (CCL) which it supplies to the DPU upon DPU request. The CCL is provided to the DPU, upon DPU request, during the DPU's boot-up sequence prior to execution of the normal DPU program. This allows for modification of DPU parameter and program. The ENDLIST command should be the last command in the CCL to indicate the end of the CCL.

The DPU status word (byte 41 of Digital Status packets and byte 18 of the DPU State Change packet) indicates the current state within the DPU boot procedure. When the DPU is initially reset, all bits in the status word will become zero. The Ground Command Enabled (GCE) bit dictates the times when ground commands can properly be handled by the DPU. As the DPU boots up (and processes the CCL), ground commands would interfere with proper parameter setting in the DPU and therefore the POCC should refrain from sending of ground commands when the GCE is set to zero.

10) ENABDATA - Enable Asynchronous Data Sources. Under any circumstances, the DPU produces a fixed amount of data consisting of housekeeping, status and low-resolution rate data. Asynchronous data items produce a variable amount of data depending on the particle fluxes present in the SAMPEX environment. This command allows for disabling of asynchronous data items to conserve bulk memory. This command requires no knowledge concerning the current state of the asynchronous data sources.

The command contains two parameters; an itemmask and a newstate. The itemmask tells which parameter settings are to be modified with choices of HILT events, LEICA events, MAST events, PET events, HILT high-resolution rates, and PET high-resolution rates. Each asynchronous data source is represented as a single bit in the itemmask so that one or many can be modified by a single command. The second parameter, newstate, indicates the desired new state for the specified items. For example, to enable HILT events and PET high-resolution rates (HRR), the command would contain parameters: itemmask=84 hex (HILT events bit set and PET HRR bit set), and newstate=1 (new state = ON). For each of the specifiable data items, a dedicated packet type is generated if associated item is enabled.

11) LVPSCNTL - MAST/PET LVPS Control. This command is necessary to set the relays in the MAST/PET LVPS. The first parameter, itemmask, dictates which of the relays should be operated. The second parameter, newstate, tells the desired new state of the specified relays. If more than one itemmask bit is set, the relays will be operated by the DPU in the order: MAST, PET, and then Oscillator,. It is important to note that there is no Oscillator OFF command to the LVPS and therefore a request of the type to the DPU will be ignored.

12) HILTVALV - HILT Valve and Cover Control. This command allows for opening and closing of the HILT valve and cover. The first two parameters of the command specify the items to operate and the direction of movement. To open a particular valve, for instance, set it's bit in the itemmask and set the newstate value to 1 indicating that the item should be opened. Due to the current required to move a valve, only a single valve will be operated at a time under DPU control. If the command specifies that several valves be operated, then the priority order for service is: Main Valve, Vent Valve, Flow Regulation, Gas Regulation, Cover Control.

Most of the HILT valve provide feedback to the DPU indicating the state of the valve, including OPEN, CLOSE, or neither. The timeout parameter specifies the maximum length of time to spend on a particular valve in case it doesn't come to rest at the desired state according to the feedback provided.

13) HILTHVEN - HILT High-Voltage Enable. The HILT sensor has three high-

voltage enable lines controlled by the DPU which are referred to as SSD HV, Drift HV, and PC Bias HV. The first two parameters of the HILTHVEN command, namely itemmask and newstate, provide a method for setting the desired state of the high voltages to either enabled or disabled. None of the high-voltages will actually be enabled unless the pressure monitor (from HILT) indicates that the pressure is above 60 Torr.

The PC Bias HV can be disabled by one more level of safe-guarding. The last 3 parameters of the HILTHVEN command specify the condition at which the PC Bias HV should automatically be shut off. The ssditem parameter specifies the parameter to be compared for the threshold condition with options of SSD1, SSD2, SSD3, and SSD4 which will be referred to as SSDn to complete this discussion. Parameter 4 specifies ln(PCFE) and parameter 5 specifies ln(SSDn) of which PCFE and SSDITEM are the actual threshold setting. The PC Bias HV is disabled if ($PCFE_{measured} > PCFE_{threshold}$) .and. ($SSDn_{measured} < SSD_{threshold}$). This assumes that the PC Bias HV has been enabled with parameters 1 and 2, and that the pressure monitor also allows enabling of the PC Bias.

14) READHILT - Read EEPROM/LCA Memory. This command forces the readout of HILT's EEPROM memory or LCA. The mask byte indicates which of LCA Unit Select, LCA Readback, LCA Masked, LCA Compare, or EEPROM are to be read. The starting address and length fields describe completely the block of data which is to be output and both the address and length fields must be supplied as multiples of 8. Each 256-byte segment (or portion thereof) will be packetized by the DPU to form a EEPROM/LCA Memory Dump packet. Packets will be output by the DPU until an amount of dump data equal to or exceeding the length field is met. The DPU reads 8 bytes of EEPROM/LCA data from the HILT each second, and therefore 64 seconds would be required by the DPU to compose a single EEPROM/LCA Memory Dump packet.

15) SETHADDR - Set EEPROM/LCA Starting Address for Write. This command is used to set the starting address for an overwrite of the HILT EEPROM. It is used in conjunction with the WRITHILT command to actually modify the EEPROM contents permanently.

16) WRITHILT - Write EEPROM/LCA Data. This commands allows for overwriting of the HILT EEPROM memory when used in conjunction with the SETHADDR command. If we desire to overwrite 12 bytes (overwrite data is 11, 22, ..., CC for this example) of EEPROM memory starting at location 100, the following sequence of commands would be sent:

6a) SETHADDR, starting address=100.

6b) WRITHILT, data1=11, data2=22, data3=33, data4=44, BLKCTRL=1

6c) WRITHILT, data1=55, data2=66, data3=77, data4=88, BLKCTRL=1

6d) WRITHILT, data1=99, data2=AA, data3=BB, data4=CC, BLKCTRL=0

Notice that the overwrite pointer is automatically incremented by four after the execution of each WRITHILT command, and therefore the SETHADDR address does not need to be resent after each WRITHILT command. Also notice that the BLKCTRL value is used to show that last of a block write and should be set to 0 on the last WRITHILT command of a block.

17) HLORBIT - HILT/LEICA Event Memory Allocation per Orbit. As described for the ENABDATA (DPU command 10) command, the DPU receives and packetizes several asynchronous data item types from the four instruments. This command, and several which follow, are designed to govern the output rate to bulk memory for each of the asynchronous data items. This command sets the number of bytes initially allocated to each of HILT and LEICA event packets. The quotas are specified in blocks where each block is 256 bytes.

As an example, when a HILT event packet is output to the SEDS, the associated quota is decremented by the packet length. When the quota is exhausted, then the DPU will no longer output HILT event packets. At the end of the orbit (90 minutes), the DPU reclaims any unused portion of the quotas and redistributes it according to the Reallocation Percentages set with the REALLOC1 and REALLOC2 commands.

18) MPORBIT - MAST/PET Event Memory Allocation per Orbit. This command sets the number of bytes initially allocated to each of MAST and PET event packets. The quotas are specified in blocks where each block is 256 bytes. For more details and an example, see the text for the HLORBIT command.

19) HRRORBIT - High-resolution Rate Allocation per Orbit. This command functions similarly to the HLORBIT and MPORBIT commands, except that it sets the initial quota for the HILT and PET high-resolution rate packets. Otherwise, its handling is the same.

20) REALLOC1 - Set Reallocation Percentages - HILT, LEICA, MAST Events. This command sets the reallocation percentages for the HILT, LEICA, and MAST events packets. As mentioned in the HLORBIT command description, the DPU reclaims unused quota at the end of each orbit and distributes it, as necessary, to the enabled data sources. Each reallocation percentage specifies a number N (range 0 to 32) which tells the amount of the memory which should be given back to that particular sensor. The actual memory calculation is N/32. All reallocation parameters (6 total in the REALLOC1 and REALLOC2 commands) should total not greater than 32 since

the data in the buffer to see if the selected parameter exceeded the threshold at any time during the interval in which case the complete packet is output. The HLTTHRES command selects the parameter to compare against as well as the threshold value.

29) STRTHIST - Start History Data Readout. This command starts the flow of history packets from the DPU and selects which packets are output. The mask parameter allows for selection of any or all of HILT, LEICA, MAST, PET or the DPU by providing a separate bit to select the readout from each. After receiving this command, the DPU will output 1 history packet each second until the total requested have been output. The order of readout is HILT, LEICA, MAST, PET, and then the DPU in case all are selected. The following list shows the number of packet for each source:

HILT - 5 packets
LEICA - 4 packets
MAST - 5 packets
PET - 4 packets
DPU - 1 packet

The maximum total number of packets output is 19, and therefore the maximum time to output all history data is 19 seconds.

30) PARAMDMP - Dump DPU Parameter Area. This command forces the DPU to output a DPU Parameter Dump packet including the current settings of all DPU commandable parameters.

31) RSTCNTRS - Reset DPU Command Counters. The DPU maintains four command counters: Time Command Count, Time Command Error Count, General (non-time) Command Count, and General Command Error Count. This command forces all four DPU command counters to zero.

32) RSTQUOTAS - Restart Memory Quotas. DPU commands 17 thru 21 describe the orbit-based quota system used in the DPU to govern the amount of event and high-resolution data output to the SEDS. As mentioned in the REALLOC1 command, the unused quota for one orbit is redistributed over the next orbit as necessary to meet the sensor requirements. The RSTQUOTAS command is used to force the quota system to zero the unused quota counter so that the entire operation can be started cleanly when the orbit quotas or reallocation percentages are modified.

This command must be transmitted to the DPU following any of HLORBIT, MPORBIT, HRRORBIT, HILT1SEC, LEIC1SEC, MAST1SEC or PET1SEC to make the quota change take effect.

33) HILTRLY - HILT Power Relay. The HILT preregulator board housed within the DPU enclosure contains a relay for power distribution to the HILT sensor. If the