

THE SAMPEX DATA PROCESSING UNIT (DPU)

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Introduction

The Data Processing Unit (DPU) serves as the interconnection between the four sensor payload and the Small Explorer Data System (SEDS). The DPU is based on the Harris 80C85RH microprocessor and includes 24 Kbytes of PROM and 56 Kbytes RAM. Actel Field Programmable Gate Arrays (FPGAs) are utilized to gain a high degree of parallel hardware processing, redundancy, and fault tolerance without the penalty of greatly increased power or weight. The DPU box, including preregulators for the HILT and LEICA sensors, measures 7" (L) x 7" (W) x 9.7" (H) and weighs 7.01 lbs.

The DPU philosophy for SAMPEX was to provide a single power and data interface to the spacecraft for the instrument payload. Figure 1 shows a system connection block diagram for the sensors, DPU, and the SEDS. The DPU provides timing and control signals to the sensors to facilitate data acquisition and mode switching while combining sensor and DPU data to form telemetry packets which are transmitted to the SEDS for recorder storage. Data received by the DPU from all instruments are similar in type, however the controls and timing necessary to read data differs between instruments based on the dissimilar heritages of the sensors. All ground commands, whether destined for the DPU or one of the sensors, are passed through the DPU where the command checksum can be verified prior to actual command execution.

Sensor Data Items

The four sensors of the SAMPEX payload share similar data type outputs even though the method for accessing the data differs between sensors. A brief description of the common sensor data types is given below.

Analog Housekeeping - The SAMPEX instrument payload (and DPU) contains 79 analog items comprised of voltage, temperature, and pressure monitors. The DPU digitizes one analog value every 0.5 seconds to produce an Analog Housekeeping telemetry packet once per minute.

Digital Status - The DPU status packet is output once per minute and contains such items as DPU state, error flags, command and error counters, sensor statuses, valve and cover statuses, high-voltage statuses, etc. Some digital status items are available within the DPU, however others must be read from the sensors before the Digital Status telemetry can be built.

Counting Rates - Sampling of counting rate data by the DPU is done at two intervals. Low-resolution rate data is read periodically and integrated to form 6-second totals. A selected subset of counters undergo special handling to produce 100 millisecond samples which provide higher resolution time sequences and give more detailed structural information for the particle fluxes involved.

Pulse Height Analyzed (PHA) Events - PHA events are output from the sensors asynchronously at a rate dependent on the particle flux incident on detectors within the sensor. The DPU reads event data items from sensors as they become available (up to 60 events/second) and produces event packets which can easily exceed the storage available in the SEDS solid-state recorder (RPP). A two tiered quota system is implemented in the DPU software to optimize the use of the recorder by throttling packet storage of incoming event data. A detailed description of the quota system is described below.

Operational Requirements

The primary function of the DPU is to collect all data items mentioned above to create telemetry packets for transmission to the solid-state recorder located within the SEDS. The 22 Mbyte recorder is dumped twice per day, therefore allowing an average data rate of 4.271 Kbits/sec, but supporting up to 100 Kbits/sec for burst mode operations. Due to the potentially high telemetry bandwidth that may be required for the storage of event data during a solar flare for instance, the DPU performs algorithms which maximize the utilization of the solid-state recorder memory while simultaneously attempting to protect against premature recorder fill-up following a ground pass.

The DPU must provide several control functions for the sensors to facilitate data acquisition and mode switching. The MAST sensor requires a controlword (simulated sector information) from the DPU every 750 milliseconds to support internal rate multiplexing and calibration support. Similar functions are provided for the PET sensor except that controlwords are needed at 50 millisecond intervals to support high-resolution counting rate data collection. The MAST and PET configuration hardware relies on a series of commandwords (6 for MAST, 3 for PET) which are supplied from the DPU. Operationally, the DPU repeatedly cycles through these commandwords, transmitting one per second per sensor to protect against single-event-upset within the sensor. The DPU performs analog multiplexing and time distribution at 1 second intervals for the LEICA sensor.

The DPU is more intimately connected to the HILT sensor where it controls, through Hall sensor feedbacks, open/close operations for the aperture cover and isobutane control valves. In addition, the DPU performs continuous isobutane pressure monitoring for safing of the high voltage system, distributes time for PHA event timetagging, and provides both multiplexer and event selection control. The DPU also monitors HILT XILINX status messages and computes 16-bit CRC checksums for the HILT EEPROM to see if either single-event-upset (SEU) or latch-up of the HILT digital electronics has occurred. To respond to such a condition, the DPU has both warm and cold reboot controls for the HILT digital electronics.

Command Description

Commands passing from the SEDS to the DPU consist of 64 bits each, with the last 8 bits defined as the command checksum. The checksum verifies the integrity of the command and all included parameters before execution is performed in the DPU. A total of 59 commands are recognized; one of which allows for modifying DPU code and data, therefore making modification of the DPU program post-launch possible.

Telemetry Description

The basic unit of data transferred from the DPU to the SEDS is an NSSDC standard packet consisting of a primary header (6 bytes), a secondary header (10 bytes), and a variable length data block. The DPU hardware interface transmits fixed length packets, each of length 512 bytes to the SEDS, however packets are truncated to the length specified in the secondary header by the SEDS before recorder storage is performed. Each packet contains an application ID (APID) which specifies the type of data enclosed and a 16 bit checksum which certifies the integrity of the complete packet.

Table 1 gives a list of telemetry packets produced by the DPU including characteristics specific to each type. The telemetry system of the SEDS supports two virtual channels, one for real-time data and one for data destined for the solid state recorder. Data sent to the real-time virtual channel is only available during ground passes (nominally 8 - 10 minutes / 12 hours) but forms the fastest method for assessing the health of the DPU and sensor payload. Real time packet output is enabled/disabled via ground commands issued from the Payload Operations Control Center (POCC).

The DPU utilizes three separate data compression schemes which reduce the requirement on the telemetry stream. Table 2 shows how the compression schemes are used including the maximum error which results from the data compression process.

Hardware Design

The DPU hardware design makes extensive use of Actel Field Programmable Gate Arrays (FPGAs) to implement a modular hardware system. The block diagram of the DPU shown in Figure 2 also serves as a high-level schematic to show how Actels are used to partition the design. Actel FPGAs are especially attractive for satellite instrumentation since each chip provides approximately 2000 logic gates in a quad flatpack package 2.2 cm². Power dissipation for an Actel component depends on many factors, but for the SAMPEX DPU, where a total of 12 FPGAs are used, the average power dissipation is 102.5 mW.

The Actel components afford very high density digital designs, therefore, in the SAMPEX context each sensor's complete data interface is implemented in a single chip including the logic necessary to tri-state (electrically disconnect) the sensor interface. Each sensor interface is equipped with a Direct Memory Access (DMA) capability which requires minimal CPU intervention only to start data transfer operations (i.e. fetch data block, transfer serial command, etc.). Each sensor's interface can be selectively enabled or disabled under ground control, therefore protecting the DPU in case one of the sensors encounters some type of catastrophic failure which might otherwise paralyze the DPU.

The DPU's spacecraft interface (including command, telemetry, and time distribution interfaces) is implemented within the DPU using a single Actel FPGA. Spacecraft interface redundancy is achieved by collocating two copies of the Spacecraft Interface chip on the interface board. The best of the two spacecraft interfaces is chosen during the DPU's power on diagnostics where the SEDS provides an echo feature to help with the selection process.

The Memory Mapper, also shown in Figure 2, is included in the DPU design to protect against system failure based on RAM chip or cell failure. The RAM array consists of seven 8K x 8 bit RAM chips of which only 6 are needed to perform all DPU functions. As the DPU powers on, an exhaustive memory test is performed which tests not only the RAM cells, but also address and data input lines as well. As the memory verification process proceeds, the Memory Mapper maps good chips to lower memory locations and bad or suspect chips to higher locations. The PROM version of the program/data is organized so that critical items are placed in lowest memory locations, therefore when the DPU program/data are downloaded from PROM to configured RAM, the most critical items are placed in the validated section of the RAM array. With this scheme, 1 RAM chip can fail with no impact on DPU operations; up to 3 RAMs can fail with only the loss of nonessential operations (history buffers).

Figure 3 shows a box-level mechanical schematic for the DPU box. The system consists of a total of 5 printed circuit boards each with dimensions 5.6 inches x 8.5 inches.

The board inventory consists of 1 microprocessor board, 1 sensor/spacecraft interface board, and 3 power supply boards. The power supply boards convert unregulated spacecraft power to regulated voltages usable by each of the DPU, HILT, and LEICA. Table 3 provides a mass/power breakdown for the components of the DPU box. A photograph of the sensor/spacecraft interface board is given in Figure 4 showing the high density designs made possible with the Surface Mount Technology / Vapor Phase Reflow process available in the Space and Environments Technology Center of the Aerospace Corporation.

Task Scheduling Table

Each sensor contains multiple hardware ports which support a different data type (e.g., digital status, counting rates, or PHA data), but organized so that only one type of data can be output at a time. The DPU-sensor interface is a request oriented system in that the DPU first specifies the information which it wants and then receives the data as it is output from the sensor. The DPU software must coordinate read-outs from the sensors so that all data items are read as needed for the creation of low and high-resolution rates and digital status packets while simultaneously using any available interface dead time to readout asynchronously occurring PHA event data.

In addition, the software system must schedule the creation of telemetry packets, the use of the spacecraft interfaces, and processing time for data compression or packet checksum calculation. As shown in Figure 5, the software system implements a task scheduling system which dictates when operations are performed. The task scheduler is comprised of a Task Scheduling Table (TST) and a hardware-based 10 millisecond interval timer which sets the operation interval. The TST contains a total of 100 elements, one for each 10 millisecond period within any given second. Each TST entry contains 16 bits where each bit indicates a specific function to be performed by the DPU at that time. Multiple operations can be scheduled for the same 10 millisecond slot by setting multiple bits in the TST entry. Operations which are performed less frequently than once per second require a separate auxiliary counter to postpone processing beyond the 1 second limitation of the TST.

The task scheduling scheme allows separate subroutines, each with a finite function (read counting rates, process S/C command, check HILT high voltage, reset watchdog timer, etc.), to be coded and tested independently. The TST then allows operations, whether sensor interface related or processing related, to be combined to form the final software product. Incompatible operations can be separated in time, and processor and interface hardware may be load balanced for most efficient use of system resources.

PHA Event Data Handling

The DPU maximizes the science output over the entire period between ground contacts with its use of a two-tiered quota system as shown in Figure 6. The two types of quotas maintained by the DPU are one second quotas (shown as q1 - q13) and orbit quotas (shown as Q1 - Q6). Table 4 shows the default one second quotas for both PHA packets and high resolution rate packets which will be described below. One second quotas limit the instantaneous burst rate of events from each sensor, and orbital quotas limit the memory which can be consumed by a particular sensor for event data storage in any orbit. Both types of quotas are reconfigurable through the ground commanding system.

HILT, LEICA, and MAST contain multiple event types to be processed by the DPU, whereas PET has only one type. Each event type is given a separate one second quota so that each can be separately limited with access to the telemetry output buffers. Setting the appropriate one second quota to zero results in a complete elimination of a particular event type from the telemetry stream. At the next highest level, orbit quotas limit the amount of recorder memory available to each sensor for event packet storage. When an event packet is output to the telemetry stream, the appropriate orbit quota is decremented by the length (in bytes) of the packet transmitted. If the packet's orbit quota becomes zero as a result of the decrement operation, then further packets of that type are blocked from output to the recorder for the remainder of the current orbit. At the end of each orbit (~90 minutes), the DPU performs a memory reallocation algorithm which provides additional memory to each of the 6 orbit constrained packet types.

High Resolution Rate Data Handling

The DPU supports high resolution rate (HRR) data processing for 6 HILT rates and 1 PET rate. For these items, data is read once every 100 milliseconds to produce high time resolution packets at intervals of 6 seconds and 48 seconds for HILT and PET, respectively. Figure 6 shows how high resolution orbit quotas Q5 and Q6 influence output of the HRR packets based on memory limiting conditions. In addition to the orbit quotas, separate threshold settings (T1 and T2) are maintained which cause HRR packets to be output only when the threshold condition is exceeded by at least one sample within the packet. The DPU builds both types of HRR packets continuously, and when the packet becomes full (every 6 seconds for HILT or 48 seconds for PET) the data within the packet are checked against a ground-programmable threshold to see if the packet should be output. The packet is not output if the associated orbit quota has reached zero.

Memory Reallocation

As described above, the DPU maintains 6 independent orbit quotas (Q1 - Q6) and 13 separate one second quotas (q1 - q13). Orbit quotas are set in bytes/orbit and indicate the minimum memory which must be made available for storage of the particular packet type during that orbit. The actual output frequency for PHA event packets and HRR packets depends on particle fluxes seen by the sensors and therefor may vary greatly from orbit to orbit. The memory reallocation scheme provides a method for sharing unused recorder memory from previous orbits while simultaneously providing at least the minimum baseline memory allocation for the current orbit.

Following boot-up of the DPU system or reception of a "Reset Quota" command, the DPU initializes the six running quotas with the ground-programmable baseline allocations. Upon output of a PHA event or HRR packet, the associated running quota is decremented by the packet length. Further packet outputs are blocked when the associated orbit quota reaches zero, at least until the next reallocation period is reached. When the orbit completes (approximately 90 minutes), all unused memory for the current orbit is accumulated and redistributed according to the ground programmable reallocation percentages. Assuming

that the first orbit following ground pass is 0, the orbit just completed is orbit i, and the next orbit is i+1, the new orbit quota is calculated as:

$$\text{OrbitQuota}_{(i+1)} = \text{BaselineQuota} + \sum \text{UnusedMemory}_{(0, \dots, i)} * \text{ReallocationPercent}$$

where each of the 6 throttled packets has its own ground programmable baseline quota and reallocation percentage. Table 4 shows the default reallocation percentages of the SAMPEX system at the time of launch. As the orbit quota grows, it becomes increasingly more difficult to use the extended memory with localized limiting of the one second quotas. To overcome this problem, the appropriate one second quotas are doubled if the new orbit quota becomes more than twice the baseline quota for a particular packet type.

History Packets

History packets output from the DPU include housekeeping data and counting rate summaries with coverage over a complete 90 minute orbit. History data items are intended to give quick-look orbit history for the orbit previous to the ground pass when the history data output is requested. The DPU continuously maintains a circular buffer of history items for each sensor, each including accumulated counting rates (96 second sums for MAST and PET, and 48 second sums for HILT and LEICA) in addition to key housekeeping parameters. A 32 to 16 bit compression scheme (shown in Table 2) is performed on history rate items to minimize telemetry bandwidth requirements for output of history packets which compete for the real-time 16 Kbps link.

Special Functions

Some special functions are provided by the SEDS to enhance the capabilities of the DPU. As mentioned in the hardware design section, the DPU provides completely redundant interfaces to the SEDS on both the telemetry and command interfaces. During initialization, the DPU transmits a special telemetry packet which contains an embedded DPU command (Echo Command). In response to this telemetry packet, the SEDS normally transmits the Echo Command back to the DPU on the command interface. If the

currently selected interface is fully functional, then the DPU should receive the command echo within 1 second of making the request at the telemetry interface. Operationally, the DPU waits 5 seconds and if no echo is seen or if the echo received is invalid, then the interface is assumed to be faulty. Under this condition, the DPU will switch to its redundant telemetry/command interface pair and attempt the process again. In total, the DPU will attempt each interface pair 5 times before defaulting to interface set #1.

A second special packet from the DPU allows for sharing of the SEDS EEPROM for storage of DPU parameter changes and program and data patches. The DPU contains no non-volatile RAM, therefore making modifications to the original program impossible without the use of SEDS resources. A block of relative time sequences (RTSs) in the SEDS contain DPU commands which can be sent to the DPU at the request of the DPU. During the boot process of the DPU system, it sends a Request for Bootlist telemetry packets which the SEDS interprets as a ground command. In response, the SEDS outputs as many as 100 DPU commands to change default parameters, code, or data structures. With this cooperative organization, the DPU can be reconfigured/updated by the SEDS automatically following a DPU reset even in the absence of ground communication.

Acknowledgements

Successful testing of the DPU system relied heavily on the use of robust Ground Support Equipment (GSE) for which we thank Kirk Crawford and David Lau of the Aerospace Corporation. The GSE was originally designed for testing of the DPU system, but during launch and early orbit operations of the SAMPEX mission the GSE has provided scientific data displays as well. The quick-look capabilities of the GSE system, particularly those related to the early orbit operations, were crucial for early health monitoring of the scientific payload.

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dedication to understanding the operations of the DPU and sensors so that he could design the necessary procedures for testing and operating the SAMPEX science payload while on orbit. This project is supported under NASA Cooperative Agreement 26979B.

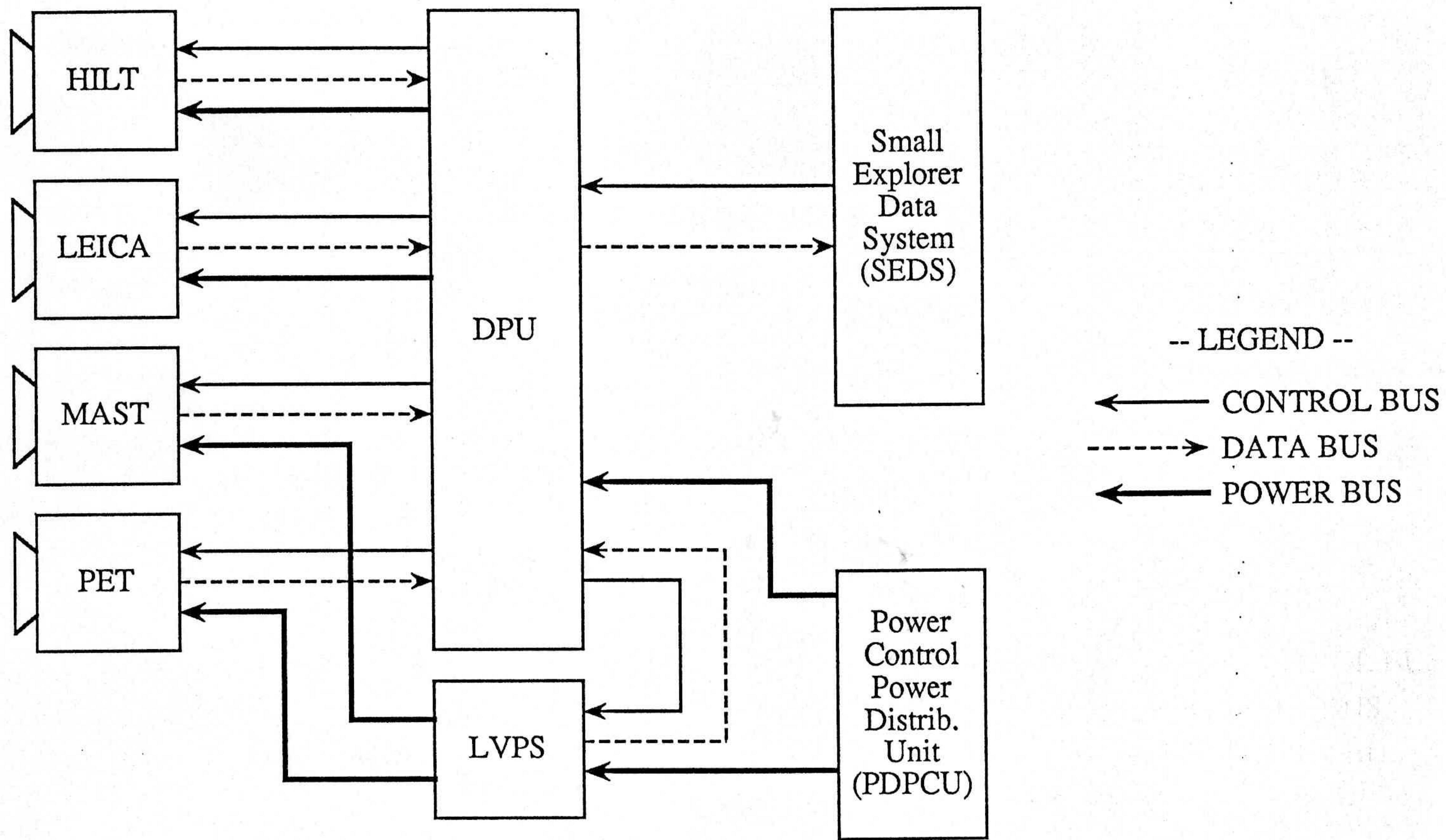
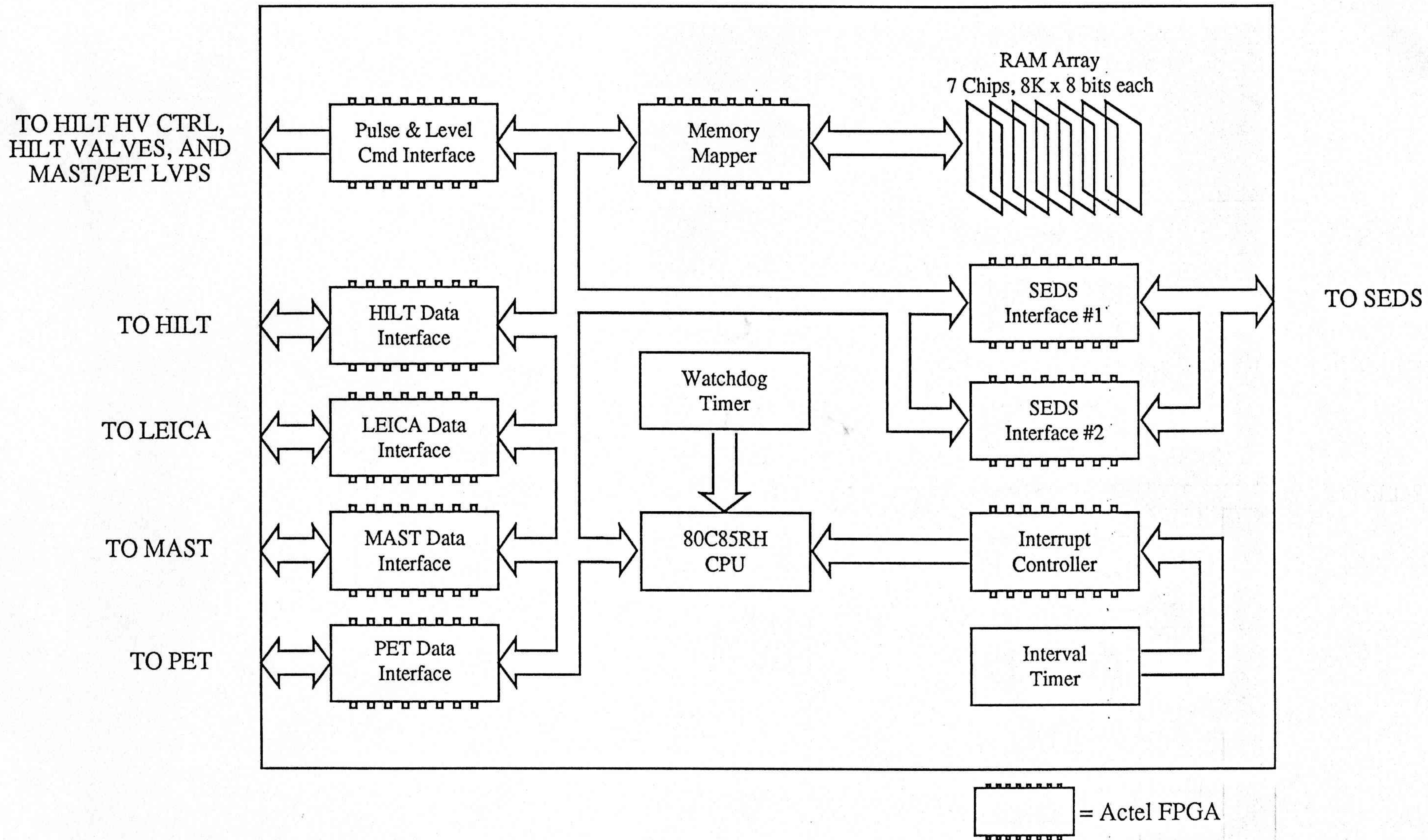


Figure 1. System Overview

Figure 2. DPU Hardware Overview



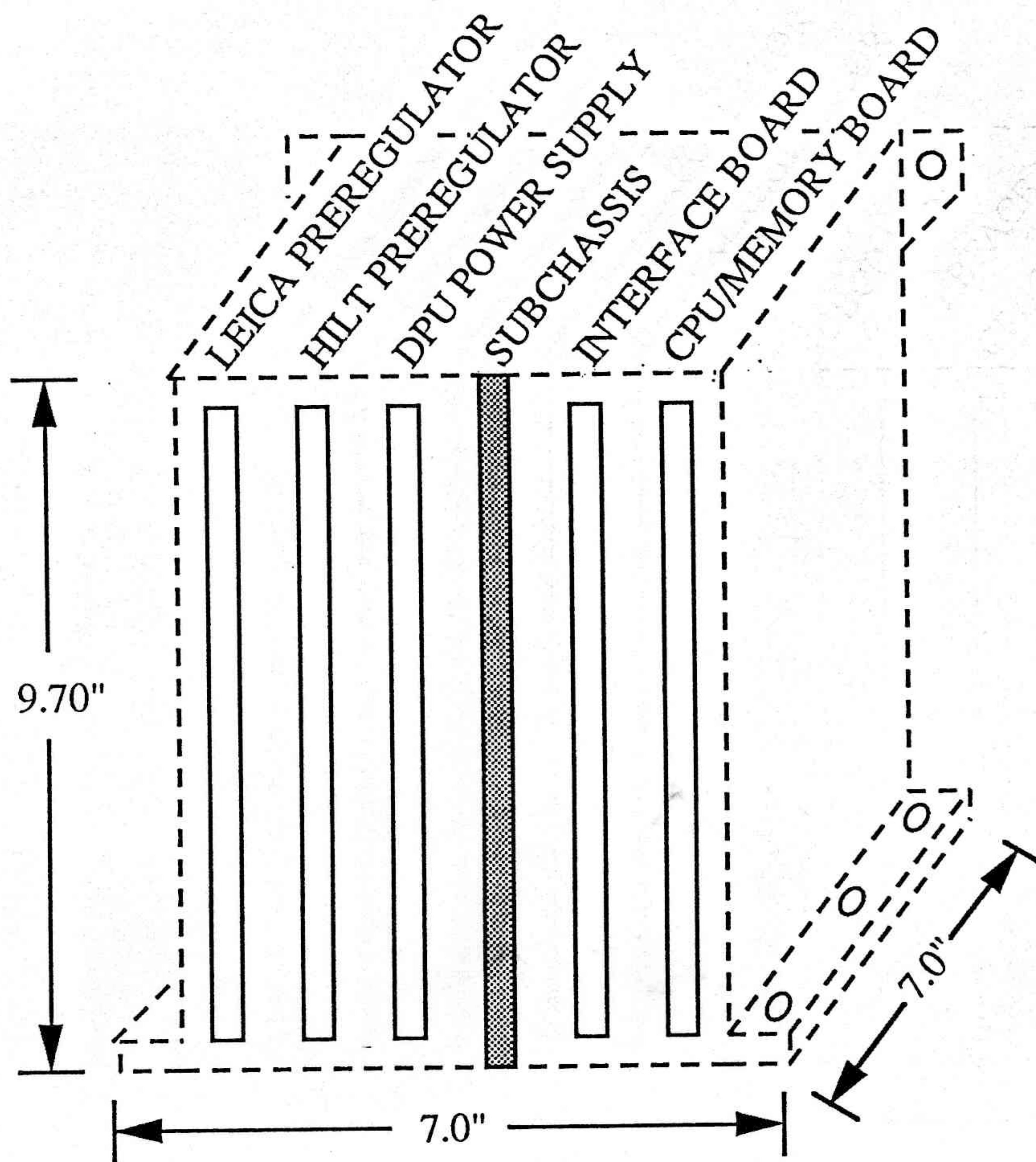


Figure 3. DPU Circuit Board Arrangement, Front View

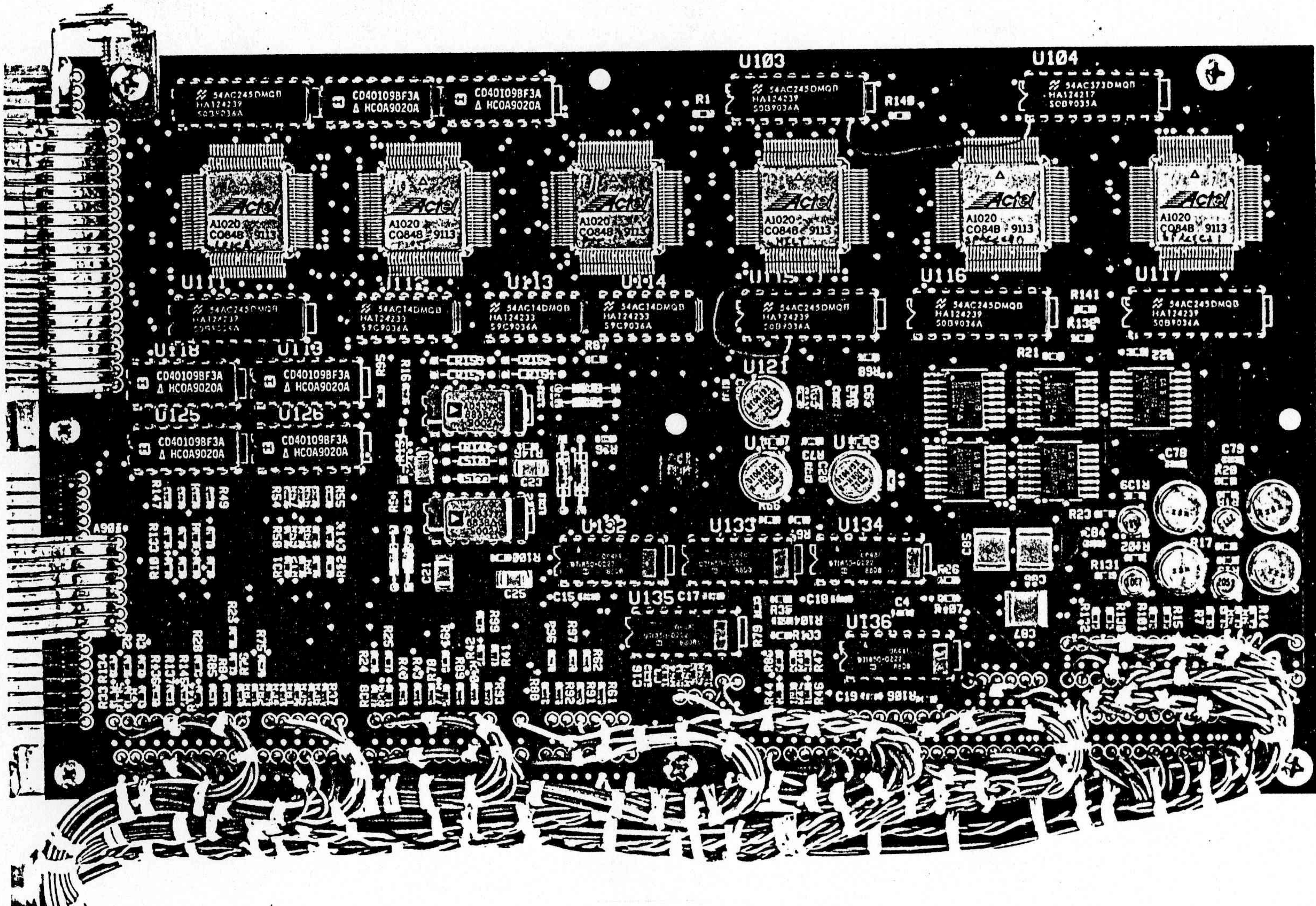


Figure 4. Sensor/Spacecraft Interface Board

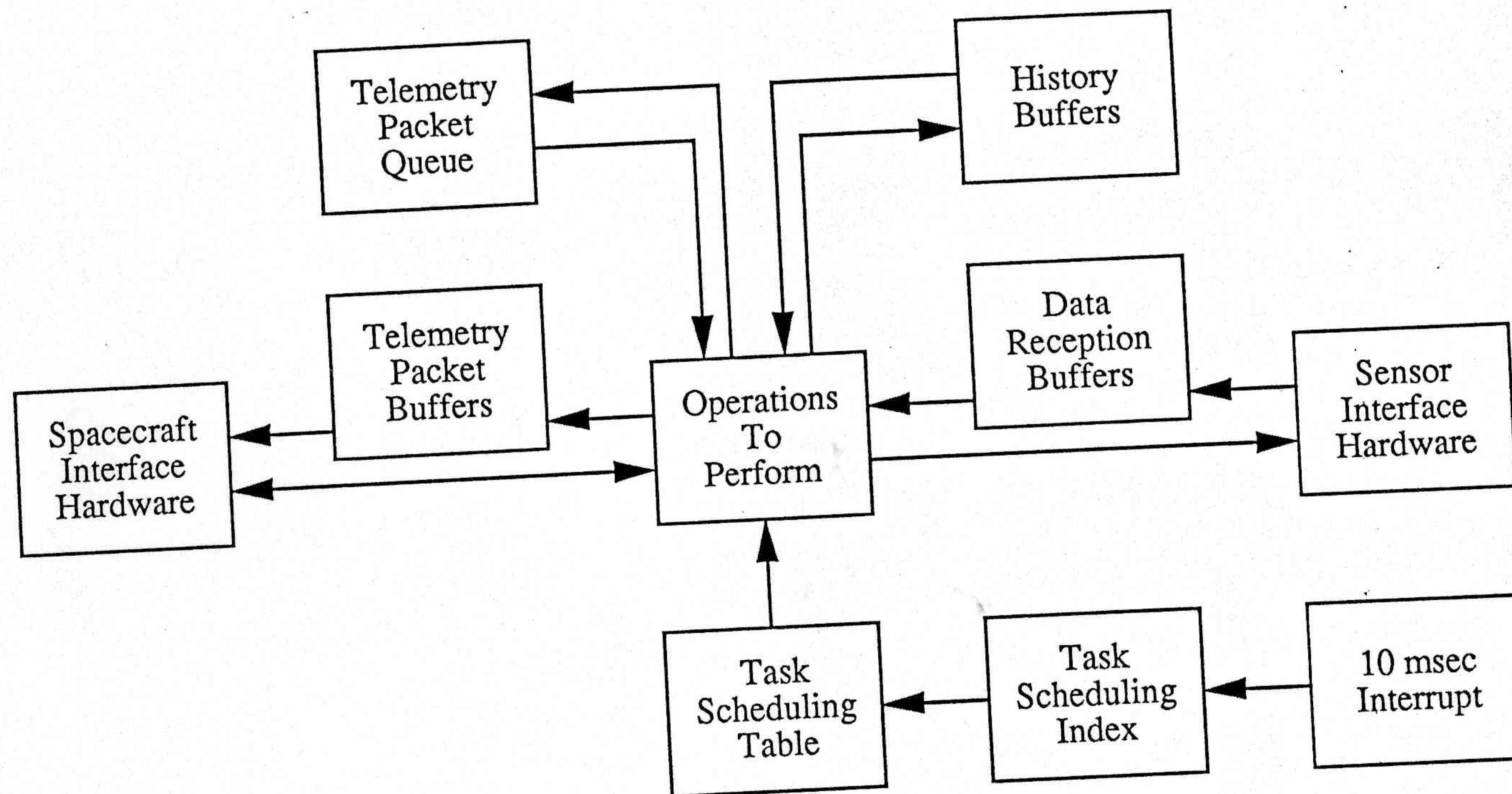


Figure 5. DPU Software System Overview

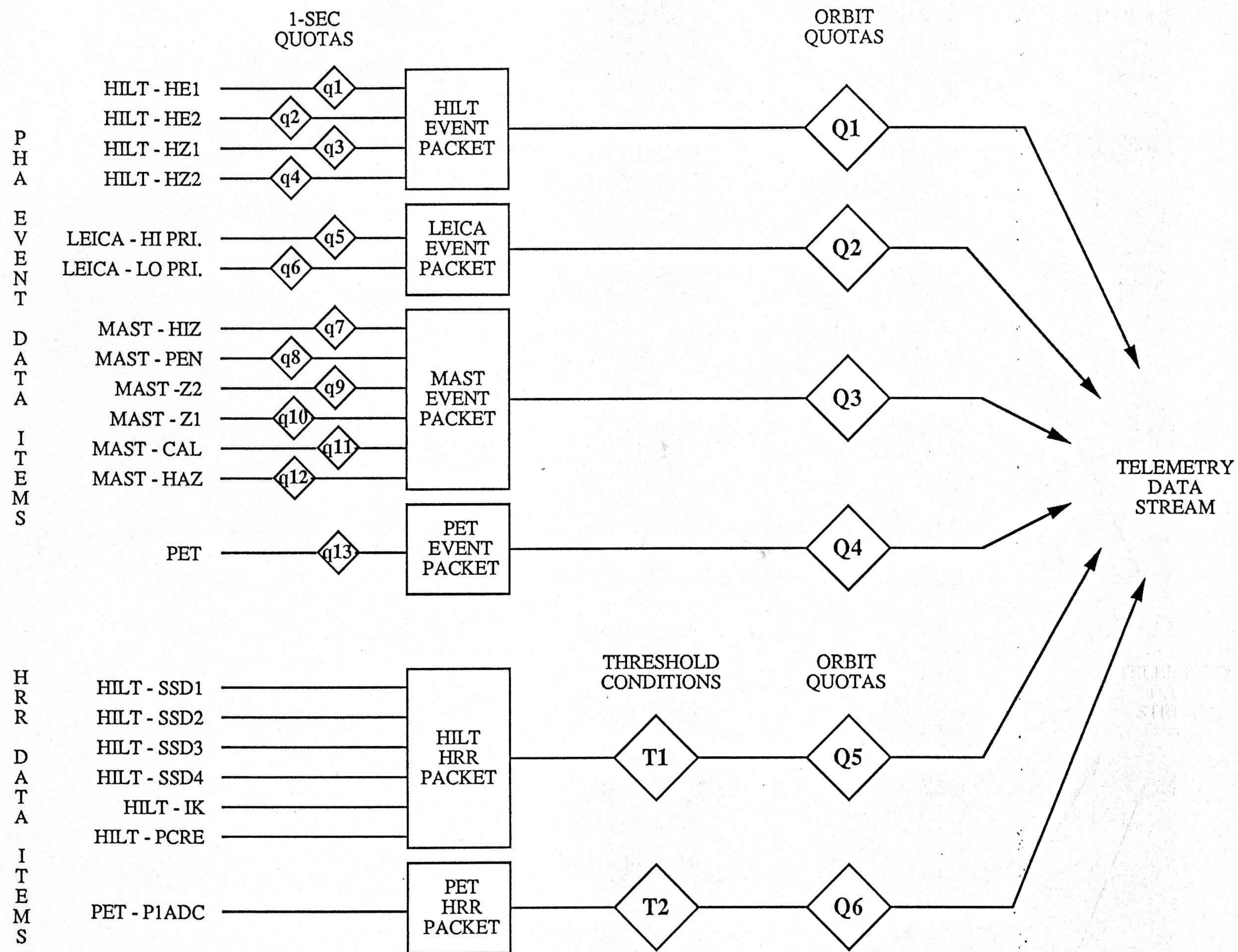


Figure 6. SAMPEX DPU Quota System

Packet Type	Application ID (APID)	Output Method	Packet Length (bytes)	Reason For Output
HILT History	33	R/T	500	Ground Command
LEICA History	34	R/T	500	Ground Command
MAST History	35	R/T	512	Ground Command
PET History	36	R/T	506	Ground Command
DPU History	37	R/T	380	Ground Command
Analog Housekeeping	38 and 42.22	R/T, Recorder	96	1 / minute
Digital Status	39 and 42.23	R/T, Recorder	122	1 / minute
DPU Command Error Echo	40 and 42.24	R/T, Recorder	30	On Cmd Error
DPU State Change	41 and 42.25	R/T, Recorder	20	During Boot
HILT PHA Event	42.0	Recorder	508 (35 events)	Packet Full or 1 hr
LEICA PHA Event	42.1	Recorder	498 (32 events)	Packet Full or 1 hr.
MAST PHA Event	42.2	Recorder	498 (20 events)	Packet Full or 256 secs.
PET PHA Event	42.3	Recorder	506 (61 events)	Packet Full or 256 secs.
HILT High-Resolution Rates	42.4	Recorder	378 (6 sec. coverage)	6 seconds if threshold met
PET High-Resolution Rates	42.5	Recorder	498 (48 sec. coverage)	48 seconds if threshold met
Low Resolution Rates	42.6 - 42.21	Recorder	90	6 seconds
DPU Parameter Dump	45 and 42.26	R/T, Recorder	60	Ground Command
EEPROM /LCA Memory Dump	43	R/T, Recorder	278	Ground Command
DPU Memory Dump	44	R/T, Recorder	276	Ground Command

R/T = Real-Time Telemetry Stream Output

Table 1. Telemetry Packets Types and Characteristics

Data Type	Input Accumulator Size (bits)	Output Mantissa Size (bits)	Output Exponent Size (bits)	Maximum Error (%)
High Resolution Rate Data (HILT & PET)	16	4	4	3.125
Low Resolution Rate Data	24	7	5	0.8
History Packet Rate Data	32	11	5	0.025

Table 2. Compression Scheme Characteristics

Table 3. DPU Mass and Power

Item	Mass (kg)	Power (W)
DPU Enclosure	1.110	-
Microprocessor Board	0.270	2.000
Interface Board	0.295	1.710
DPU Power Supply Board	0.255	0.930
HILT Preregulator Board	0.240	0.540*
LEICA Preregulator Board	0.240	0.528**
Connectors	0.571	-
Internal Harness	0.110	-
Board Mounting Hardware	0.092	-
Totals	3.183	5.708

* Assumes LEICA Instrument Power of 4.83W.

** Assumes HILT Instrument Power of 4.753W.

Data Type	Default Orbit Quota (bytes)	Default 1-Sec Quotas (Evt/sec)	Default Reallocation (%)
HILT Event Data	480,512	10	15.6
LEICA Event Data	944,896	10	31.2
MAST Event Data	944,896	10	31.2
PET Event Data	273,408	10	15.6
HILT HRR Data	126,225	-	6.2
PET HRR Data	22,950	-	0.0

Table 4. Default Quotas and Reallocation Percentages